Modelling Tunneling Currents in Ultra Thin Oxides

I. Introduction

Ever decreasing minimum geometries in MOSFET design results in a corresponding reduction in the thickness of the gate oxide. This is an inevitable result of the increasing doping levels in the channel that are required to prevent depletion from the drain becoming too high a percentage of the total device length. For these new aggressive technologies, the required ultra thin gate oxides suffer a significant oxide tunnelling component. It has therefore become important to include this component in device modelling.

For some time now, Silvaco has had models to deal with current conduction through oxides. It is only recently, however, that the number of questions to the customer support groups related to gate tunnelling effects has been increasing. It is appropriate, therefore to re-address this issue at this time.

There are two types of models in Silvaco's device simulator, *ATLAS*, which address oxide current conduction.

(i) Fowler Nordheim Tunnelling

(ii) Hot Carrier Injection.

The essential difference between these two components of current arises from from the direction of the field that is accelerating the mobile carriers.

Hot carrier injection occurs when a high local electric field exists in the same direction as the oxide/semiconductor interface. The statistics of huge numbers of free carriers travelling at high velocity results in a probability that some of them, through multiple "lucky" collisions, will attain sufficient energy to surmount the oxide/silicon energy barrier and thus enter into the oxide. Once in the oxide, electrons and holes have a low but finite mobility to move around or become trapped. This mechanism of hot carrier injection is usually studied in relation to reliability issues or for memory devices where mobile carriers in the oxide are used to to charge or discharge an isolated floating gate. Users requiring more information and worked examples on this mechanism are directed towards the "EPROM" section in the *DeckBuild* examples menu.
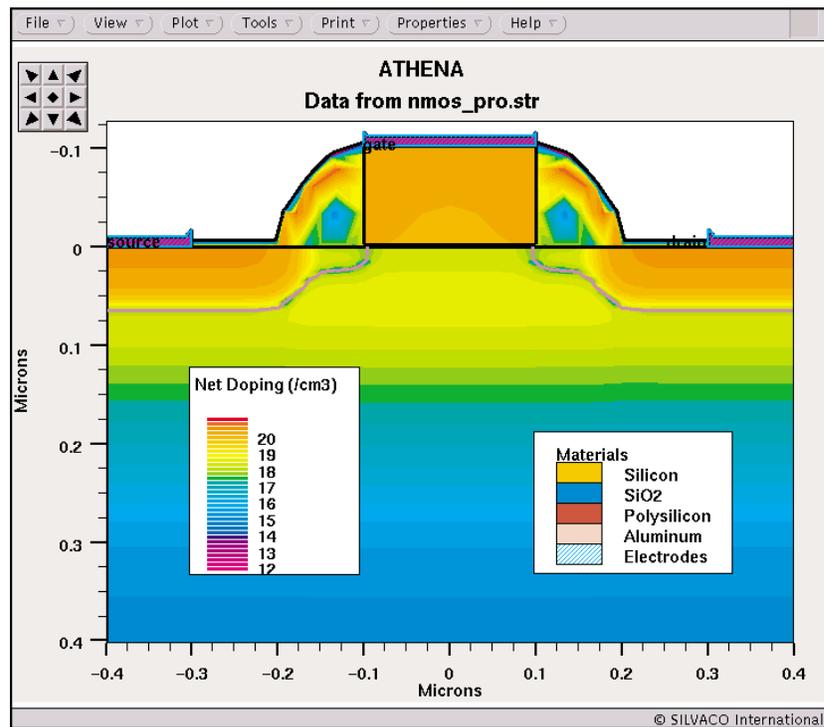

Figure 1. The typical 0.2um MOSFET with 25A gate oxide used in this example.

Fowler Nordheim tunnelling, on the other hand, arises from high local fields perpendicular to an energy barrier interface. An energy barrier interface can be induced by the presence of a semiconductor with a different band gap, in which case it is called a "hetero-junction" or it can be induced by the presence of an insulator. The insulator interface is the situation which is of most interest to silicon MOSFET designers and is the subject of this article.

II. Requirements for Modelling Tunnelling in *ATLAS*

ATLAS offers two types of model for electron or hole tunnelling that are specified in the "MODELS" statement.

(i) Post Processing Fowler Nordheim Model (FNPP)

(ii) Self Consistent Fowler Nordheim Model (FNORD)

The Post Processing model (FNPP) is a very stable model which will work for any situation. This model simply calculates the current flowing through the gate once *ATLAS* has found a solution to each solve statement and adds this current to the gate electrode. The presumption here is that the gate current is a small

Figure 2. The entire device simulation input file used in this example.

volts with a typical applied drain voltage of 50mV. The entire simulation deck is shown in Figure 2 for those who may wish to use this example as a starting point for their own device simulations. It is evident from this input file how simple it is to do these simulations.

The results of the simulation are shown in Figure 3. It is observed from these results that tunnelling current through the gate was mostly at the expense of drain current in this case. The small drain bias was applied to to demonstrate the self consistency of the solution method by monitoring the drain current.

IV. Conclusion

The Fowler Nordheim oxide tunnelling models in *ATLAS* are simple to implement and assist in the study of deep sub-micron MOSFETs gate current effects. The study here shows that for a gate oxide thickness of 25A in a typical MOSFET structure, gate oxide current can exceed the drain current for a applied gate voltages greater than 5 volts.

fraction of the total terminal currents, since clearly with this method, adding all terminal currents will no longer equal zero. For small gate leakage currents, however, this is of little consequence.

The self consistent model, FNORD, has the tunnelling equations inside the solution loop and therefore correctly calculates all terminal currents. This self consistent method, however, does require one condition for reliable convergence, namely:

> there must be a majority carrier source of the tunnelling species within a depletion width of the tunnelling oxide interface.

For most structures, such as MOSFETs, the above requirement is satisfied and good convergence should ensue.

III. Worked Example

The most common situation where oxide tunnelling is modelled is for deep sub-micron MOSFETs with very thin oxides. Figure 1 shows a typical MOSFET created using the process models in *ATHENA*. To exaggerate the effect of oxide tunnelling, a gate oxide of 25A nominal thickness was grown. The structure called "nmos_pro.str" was then imported into *ATLAS* and the gate oxide ramped to a voltage of 5.4
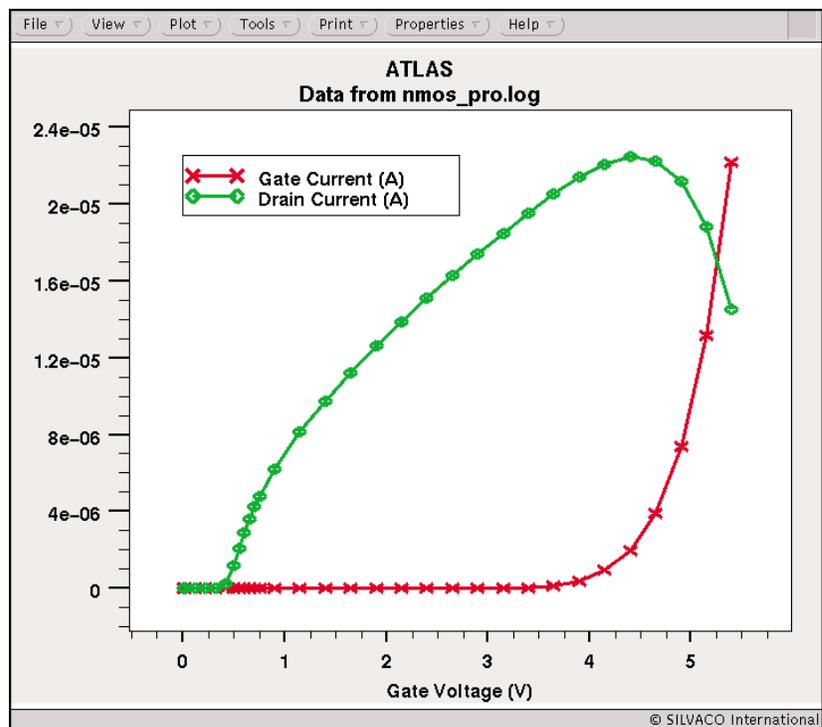

Figure 3. The simulated gate and drain currents of the device shown in Figure 1 demonstrating the self consistent Fowler Nordheim oxide tunnelling model in *ATLAS*.