Simulation Standard

TCAD Driven CAD

A Journal for Process and Device Engineers

The Industry Standard of SOI Technology From Process To Circuit Simulation

Abstract

SOI technology for state of the art CMOS technology is rapidly approaching maturity. PD-SOI device design has the advantage of easier manufacturing but requires more sophisticated device and circuit design to reduce the effects of the floating-body. FD-SOI device design potentially has the advantage of no floating-body effects but requires very thin silicon films making manufacturing more challenging. As a consequence the optimization of SOI device design requires a coupled solution where both process and circuit simulation can be tied together. Silvaco provides a complete, well integrated simulation software for all aspects of SOI technology. Our SOI specific software includes technology simulation, SPICE model extraction, interconnect parasitic analysis, SPICE circuit simulation and traditional CAD. The ***TCAD Driven CAD*** approach provides the most accurate models for both device engineers and circuit designers.

1 Introduction

The continuing trend for high speed circuits has resulted in a market increase in the application of Silicon-On-Insulator (SOI) MOSFETs. Consequently a number of phenomena, such as the presence of floating body effect, carrier heating and non-localized transport, have acquired a lot of importance in the field of semiconductor modeling. Not only they are interesting from a theoretical point of view but also play a relevant role in the functioning of devices and circuits and for this reason, need to be simulated very accurately. In this paper we will show how Silvaco's software simulator now accounts for all the specific SOI related physics from process technology simulation to circuit level including interconnect parasitics extraction.

2 Technology Simulation

The ***ATHENA*** and ***ATLAS*** simulators allow device engineers to study deep sub-micron physical effects in SOI devices. Technology simulation includes models for simulation of both fully and partially depleted SOI transistors based on accurate process geometry and doping profiles. ***ATHENA*** can model local oxidation to form silicon islands (Figure 1), shallow implant, RTA diffusion process steps and physical etching. ***ATLAS*** provides among common models for BULK and SOI technologies, the following SOI specific device simulation features: Impact Ionization model for breakdown and kink effect, self heating model for negative differential resistance simulation (Figure 2).

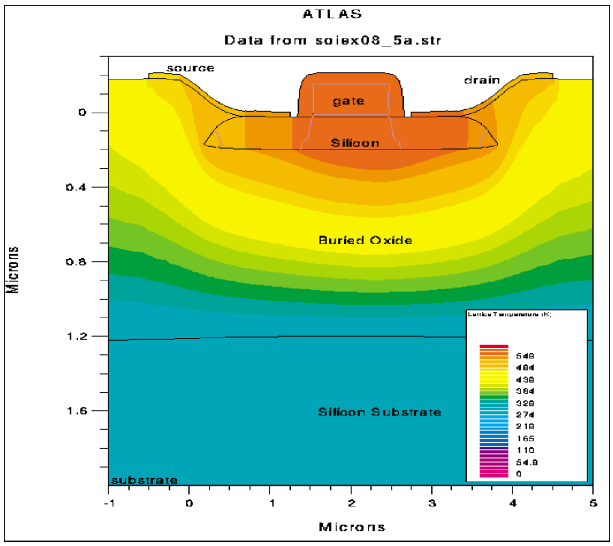

Figure 1. Short channel SOI MOSFET created using ***ATHENA***. Local oxidation is used to isolate the active layer. Here temperature distribution is shown due to self heating.

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INSIDE

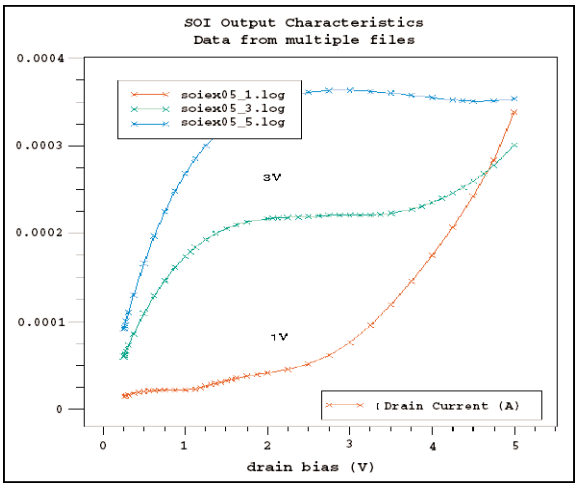

Figure 2. The impact of Self Heating is shown on Drain IV curves for SOI devices.

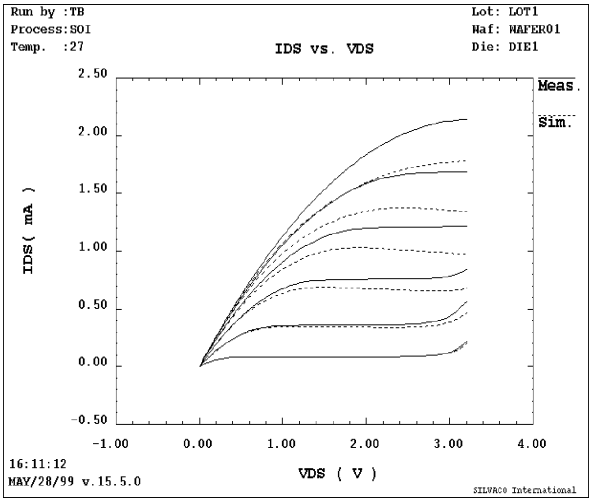

Figure 3 Global or local optimization and parameter extraction can be performed on up to 40 geometries to obtain a single scalable model.

3 Parameters Extraction

UTMOST is a complete integrated software package which provides automatic data acquisition, parameters fitting and extraction, optimization, simulation and model validation. ***UTMOST*** supports the following models: Honeywell, Florida FD and PD, STAG, BSIM3SOI (Figure 3). Thus, a complete solution is now available to fully characterize SOI devices including parasitic effects (Bipolar, diode) on either 4 or 5 terminals devices.

4 Circuit Simulator

SOI circuits pose unique problems for reliable and accurate circuit simulation. SPICE-like programs are not designed to handle negative conductances forcing designers to simulate circuits for only positive gate voltages. ***SmartSpice*** has been improved to accept any bias conditions and provide accurate and reliable SOI simulations. Some of Silvaco's fundamental improvement to BSIM3SOI model are the optimization of the Impact Ionization model and the self heating model (Figure 4).

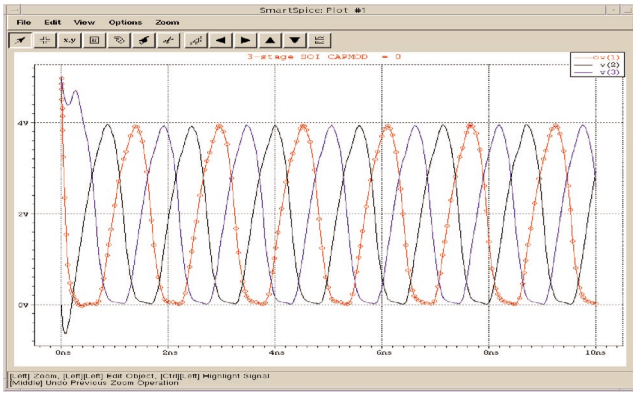

Figure 4. ***SmartSpice*** waveform from high speed digital circuit designed with fully depleted SOI devices.

5 Interconnect Parasitic Extraction from Layout

SOI devices are being used in complex deep sub-micron circuits. An accurate physical calculation of interconnect delay is important to successfully design circuit with this technology [1][2][3]. ***CLEVER*** is a physical interconnect parasitic extractor built on 3D process simulation and fast field solution techniques (Figure 5) and (Figure 6). ***CLEVER*** generates fully annotated SPICE netlist for circuit simulation (extract active devices and associated geometrical parameters (W,L,NRS,NRD,AD,PD). It can model: floating silicon islands, low-k and damascene processing, handle multiple metals and di-electrics, lithography effects including optical proximity correction and physical deposition and etch.

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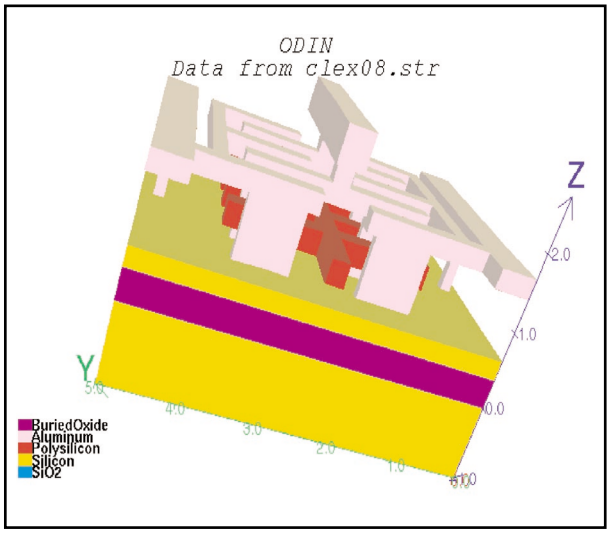

Figure 5. 3D Interconnect geometry from SOI cell layout. CLEVER applies a field solver to the 3D structure to calculate parasitics from the interconnect.

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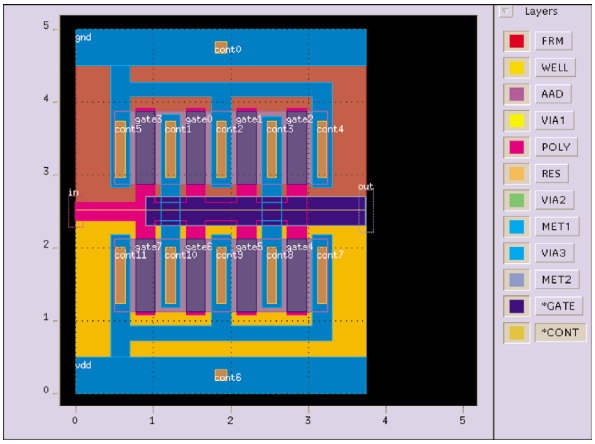

Figure 6. SOI cell layout from which 3D back end process simulation is based.

Conclusion

It has been shown that Silvaco's software is able to simulate and predict adequately state of the art SOI technology from process to circuit simulation.

References

[1] B.Froment et al,, "New interconnect capacitance characterization method for mutilevel CMOS processes" IITC 1999.

[2] Gilles Lecarval et al, 'Advanced Intercoonect Scheme Analysis: Real Impact of Technological Improvements" IEDM 1998

[1] B.Froment et al, "Ultra Low capacitance measurements in Multilevel metallisation CMOS by using q built-in Electronmeter" IEDM1999.