Simulation Standard

TCAD Driven CAD

A Journal for Process and Device Engineers

Very Low Energy Boron Implant Simulation Using New BCA Monte-Carlo Model

I. Introduction

ATHENA version 5.0 includes a new Binary Collision Algorithm (BCA) for accurate Monte-Carlo implant modeling down to sub-1keV energies. This new BCA code is a 3D model that takes account of channeling in all possible crystal directions, not just the vertical direction. Accurate modeling of all channeling directions becomes an important factor for low energy implants such as is used by the new generation of very deep submicron devices.

Typically for MOSFET applications using <100> silicon substrates and very low energy boron channel implants, in addition to channeling in the vertical direction, channeling also occurs in the <110> directions which includes a channeling direction along the surface of the crystal as shown in Figure 1.

This simulation assumed a 10A (1nm) native oxide on the surface and simulated all the implanted ions being implanted at the center point using a vertical beam with a simulated beam spread angle of ± 1 degree.

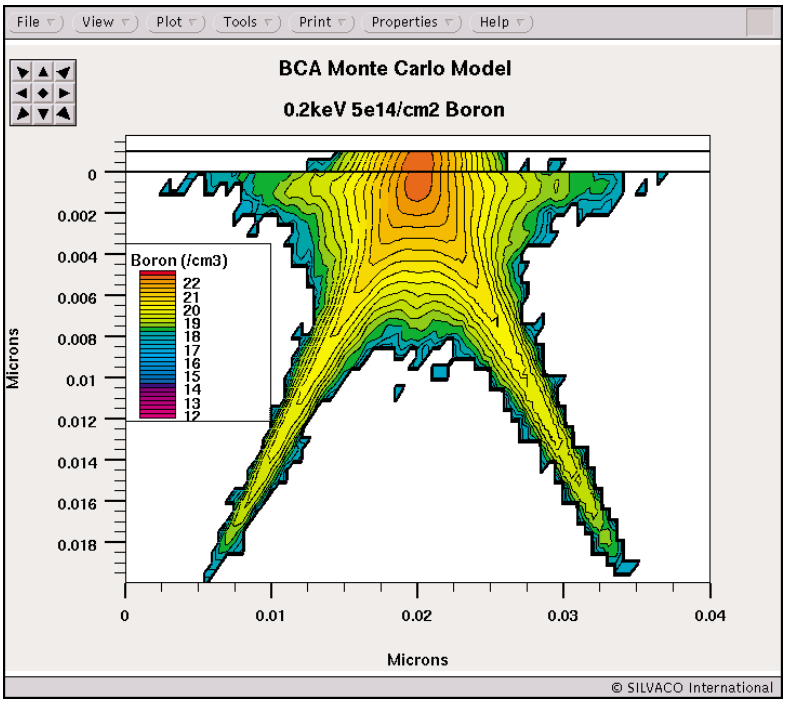

Figure 1. A point impact implant of 0.2keV boron to demonstrate channeling along the <110> planes

II. Measured Data

The output of the model was compared with published data from two separate SIMS studies using Implanters from Applied Materials and Eaton. The measured SIMS data is described in table 1.

The purpose of the germanium implants of 1keV and below was to pre-amorphise the surface layer of silicon to compare the profiles of the channeled data with non-channeled data. For energies of 1keV and above, another unspecified method was used to amorphise to a greater depth to prevent channeling.

The measured data showed several key features that were verified using the new BCA code.

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INSIDE

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Implanter	Species	Energy (keV)	Dose (/cm2)	Angle (Deg)	Substrate
Applied	B	0.2	5e14	zero	crystal
Applied	B	0.2	5e14	7	crystal
Applied	Ge / B	5 / 0.2	1e15 / 5e14	zero	crystal
Applied	B	0.5	5e14	zero	crystal
Applied	B	0.5	5e14	7	crystal
Applied	Ge / B	5 / 0.5	1e15 / 5e14	zero	crystal
Applied	B	1.0	5e14	zero	crystal
Applied	B	1.0	5e14	7	crystal
Applied	Ge / B	5 / 1.0	1e15 / 5e14	zero	crystal
Applied	B	1.0	5e14	zero	amophized
Eaton	B	2.0	3e13	zero	crystal
Eaton	B	2.0	3e13	7	crystal
Applied	B	2.5	5e14	zero	crystal
Applied	B	2.5	5e14	7	crystal
Applied	B	2.5	5e14	zero	amophized
Applied	B	5.0	5e14	zero	crystal
Applied	B	5.0	5e14	7	crystal
Applied	B	5.0	5e14	zero	amophized
Applied	B	10.0	5e14	zero	crystal
Applied	B	10.0	5e14	7	crystal
Applied	B	10.0	5e14	zero	amophized

Table 1. Measured SIMS data from Applied and Eaton used for validating the new Binary Collision Approximation Monte Carlo model.

III. Simulations

All the simulations represented in the SIMS data above were simulated using the Binary Collision Approximation (BCA) model in ***ATHENA***. The model accurately represents the damage caused by previous BCA implantations. No special damage models are required to be specified in the input file when amorphizing with the germanium implants. The user simply implants germanium first which will amorphize the surface layer, then implants boron. The model automatically calculates the depth of the surface amorphous film is from the simulated damage profile.

In order to simulate implantation into completely amorphized silicon, a polysilicon substrate was specified rather than using self implantation of high doses and energies of silicon. Both methods would have given the same result, as the BCA model treats polysilicon material as amorphous. However using polysilicon results in a faster simulation since only one implant has to be simulated instead of two.

- the SIMS profiles of boron implanted at energies of 1keV and below showed no discernable difference between implantation at zero degrees from the vertical and at 7 degrees from the vertical.
- implantation at energies of 2keV or greater showed a progressively increasing difference between implantation at zero degrees from the vertical and at 7 degrees from the vertical.
- implantation of boron into deeply amophized substrates showed no channeling tail, even down to concentrations of 1e16/cm^3 which was approximately the detection limit of the SIMS for the experiments.
- implantation into a surface layer amorphized using 5keV Ge with a dose of 1e15/cm^2 showed tails in the profiles below concentrations of approximately 1e19/cm^3.
- implantation at 0.2keV showed no difference between implantation in crystalline material and implanting into an amorphized substrate.

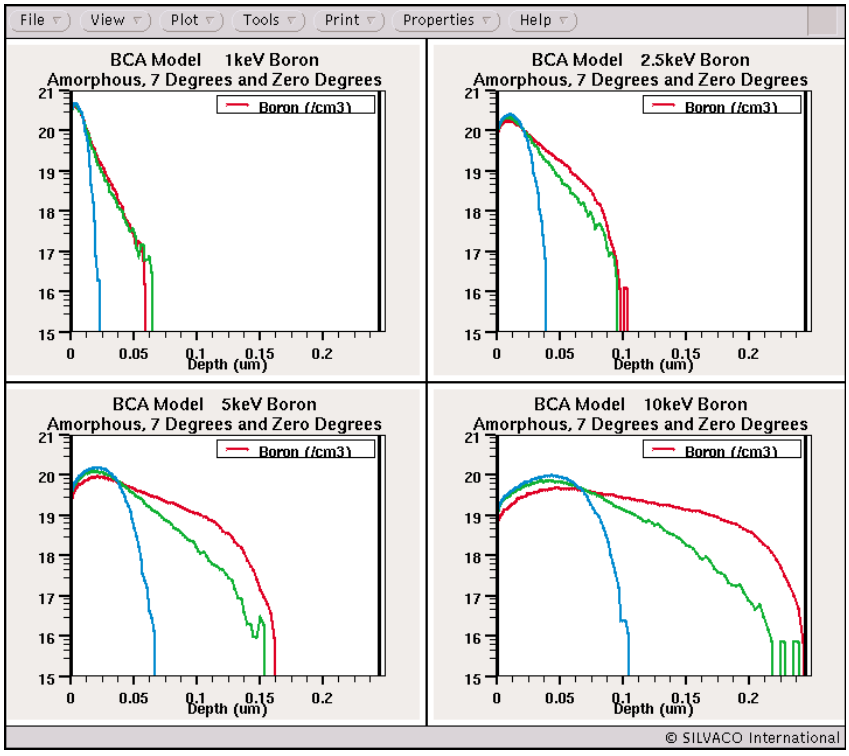

Figure 2 Simulated implants from 1keV to 10keV. The implant with the shortest range in each plot is using an amorphous silicon substrate. The implants with the medium range and longest range are into crystalline silicon at 7degrees and zero degrees repectively.

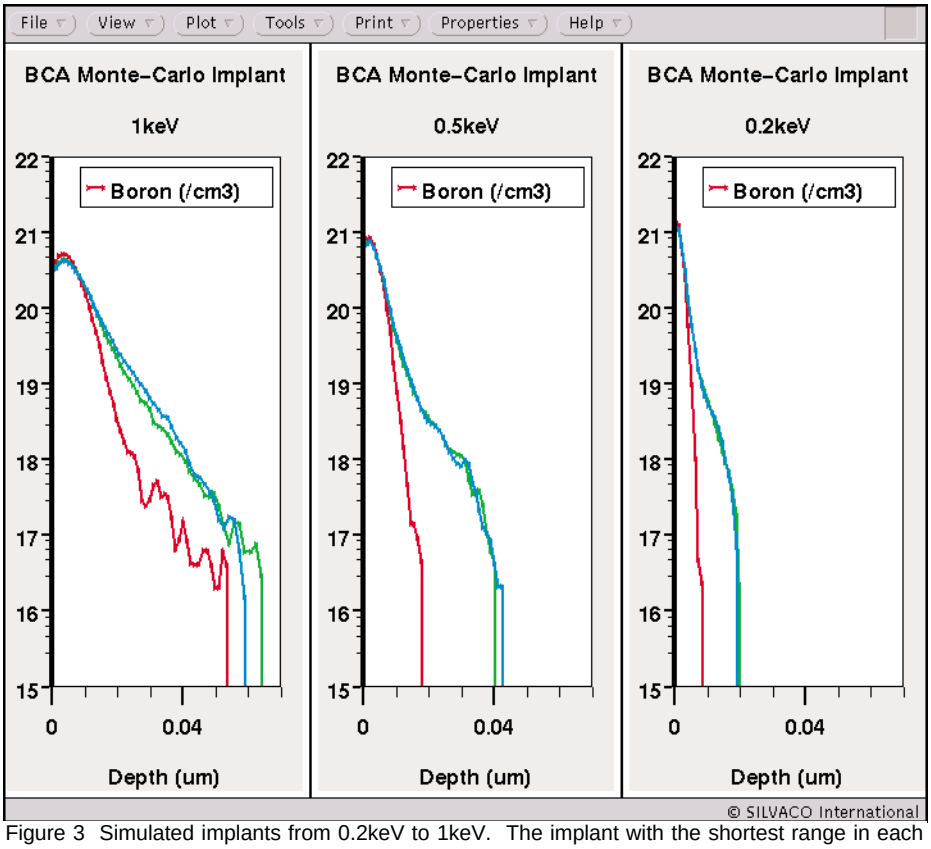

Figure 3 Simulated implants from 0.2keV to 1keV. The implant with the shortest range in each plot uses a 5keV germanium implant to pre-amorphise the surface film prior to implantation of boron. The longer range, overlapping implants are into crystal silicon at 7degrees and zero degrees repectively.

In the simulations a native oxide of 10 Angstroms (1nm) was assumed and a beam angle spread of $\pm$ 0.1 degrees.

(a) Simulations from 1keV to 10keV

Figure 2 shows simulations from 1keV to 10keV where the channeled profiles at implant angles of zero and 7 degrees are compared with simulations of a deeply amorphized substrate.

All the simulations in figure 2 show excellent agreement with the measured results both in form and absolute values. The implants at 1keV show little difference between implant angles of zero degrees and 7 degrees as shown by the measured data. At 2.5keV, differences between the two implant angles emerge, with an increasing difference at higher energies in the same manner as the SIMS data.

It is interesting to note the form of the implants into truly amorphous material. These amorphous implants all show a similar sharp cut off at the end of range of the implant both in the simulations and in the measured data. This point is highlighted as it is relevant to the discussion of the lower energy implants that follows.

(b Simulations from 0.2keV to 1keV

Figure 3 shows low energy implants from 0.2keV to 1keV. In these simulations, the "non channeled" implants were not implanted into a deep amorphous surface film as before but in this case only the top surface film was amorphized by implanting 1e15/cm^2 germanium at 5keV. If the 1keV "non channeled" data from this method is compared to the 1keV "non channeled" data obtained by implanting into a deep amorphous film, there is a difference in the tail of the implant profile, exactly as there is in the measured SIMS data.

Examination of the tail of the implant in the case where surface amorphization was created by implanting 5keV germanium shows a second point of inflection which is characteristic of channeling in this region. Implantation into a truly amorphous film results in a sharp cut off in the tail of the implant without a secondary point of inflection in the curve at the tail.

The reason the two 1keV "non channeled" data are different is because the 5keV germanium implant creates an amorphous surface film that is less than 100A (10nm) thick. Figure 4 shows the geranium implant profile. This is significantly less than the total depth of the amorphous profile of 1keV and so some channeling occurs in the tail of the implant.

Once again, the channeled data implanted at angles of zero and 7 degrees from the vertical (these overlay at energies below 1keV) showed good correlation with the measured SIMS data.

The only point of contention between the measured data and the simulated data is in the very low energy implant of 0.2keV. The measured data shows little difference between implantation into the germanium amorphized film and the channeled data. It might be suggested that because at very low energies the boron implant itself amorphises the film. The Monte-Carlo

physics suggests that this might not to be the case. A possible explanation of the measured data is that the resolution limit of the SIMS profiling technique was reached. Further evidence that this is the case is suggested by the facts that:

(i) all the measured SIMS data for 0.2keV correspond to the channeled data in the simulations.

(ii) the measured data shows a clear secondary point of inflection in the tail which suggests that the vertical resolution limit approximated to the channeled data at 0.2keV as opposed to the non channeled data.

(iii) there is little difference in the measured data versus depth between the tail of the profiles at 0.2keV and the corresponding profile of the tails of the profile of the 0.5keV implant into the surface amorphized implant.

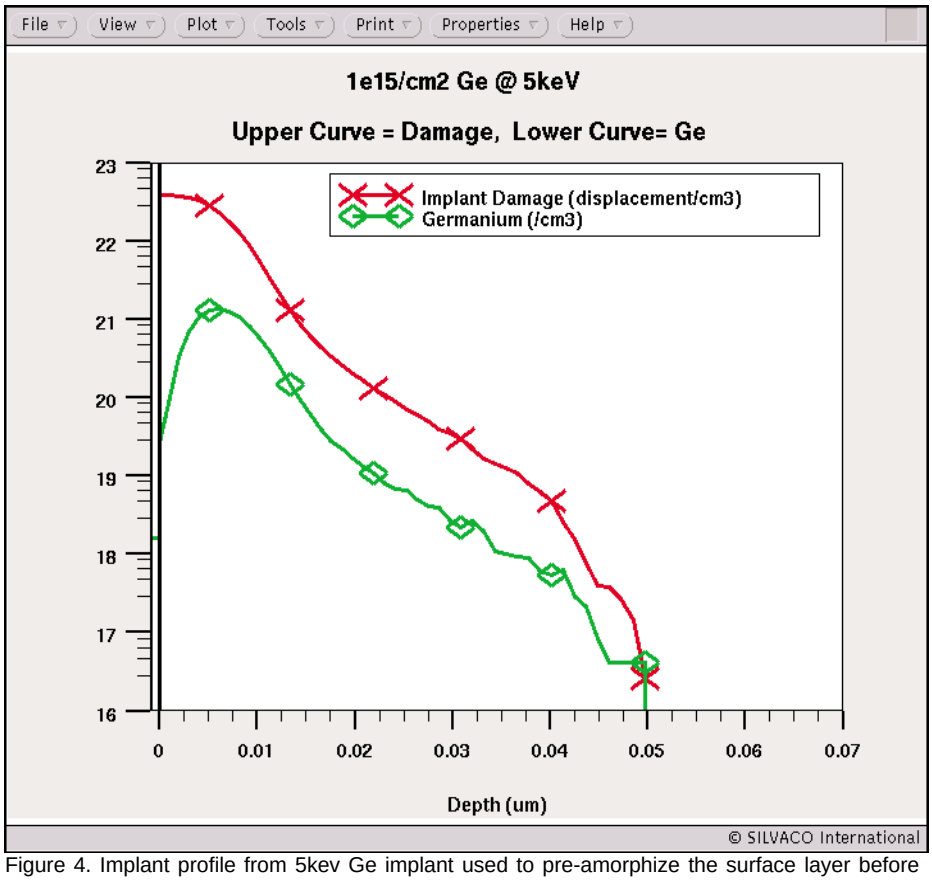

Figure 4. Implant profile from 5kev Ge implant used to pre-amorphize the surface layer before the low energy boron implants. The implant damage (which is distinct from point defect concentration) is also shown. Amorphization takes place when the damage reaches 50-60% of the substrate atomic concentration

IV. Conclusion

In conclusion the new Binary Collision Approximation implant model in ***ATHENA*** gives highly accurate results for low energy implants. A discrepancy between measured and simulated data at 0.2keV for implantation into a pre-amorphized surface film can only be resolved with repeated measurements with a better resolution limit.

To summarize, both measured and simulated data show that:

- boron implanted at energies of 1keV and below show no discernable difference between implantation at zero degrees from the vertical and at 7 degrees from the vertical.
- implantation at energies of 2keV and greater showed a progressively increasing difference between implantation at zero degrees from the vertical and at 7 degrees from the vertical as the implant energy increases.
- implantation of boron into deeply amorphied substrates invariably showed a sharp cut off of dose with distance near the end of range of the implant, regardless of implant energy. Any tail in this region is therefore strong evidence of channeling.
- implantation into a surface layer amorphized using 5keV Ge with a dose of 1e15/cm2 showed tails in the profiles which is strong evidence of channeling. 5keV germanium is therefore not sufficient to prevent channeling of implants above energies of 0.2keV.

Continous Trap Model for Accurate Device Simulation of Polysilicon TFTs

System on a Panel Requirements

There has been a significant increase in the popularity of liquid crystal displays with control circuitry being placed on to the glass (system on a panel). This has been made possible by the technological improvements of thin-film-transistors (TFTs) manufactured on glass substrates. The sudden popularity is a result of the move away from the traditional use of amorphous silicon towards polycrystalline silicon. The increase in performance by this switch has allowed these TFTs to be applied to applications beyond pixel control transistors.

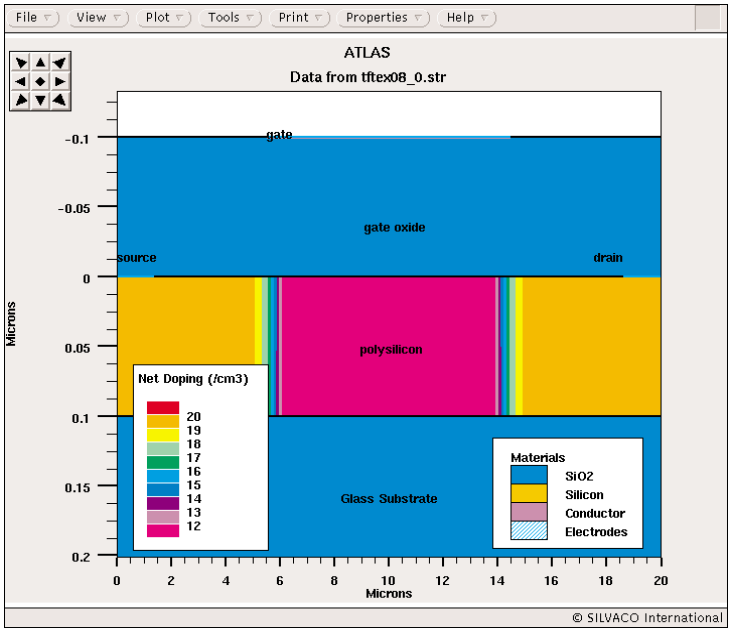

Figure 1. Geometry and doping profile of the Polysilicon TFT to be simulated.

In order to design circuits using TFTs it is fundamentally necessary to understand the physics involved in their operation. The best way of achieving this is through two-dimensional device simulation. Polysilicon consists of a number of grain and grain boundary regions. Improvements in processing have resulted in quite large, ~0.5um, well controlled grain regions. Within the grain boundaries there exists trapped charge which act as potential barriers. The effect of the trapped charge can then be modeled by defining the average band bending which is determined by the spatially averaged trapped charge density. By this means it is possible to calculate a continuous, volume averaged, density of states (DOS) profile across the band gap. This DOS profile is modeled using profiles of acceptor-like and donor-like traps distributed across the bandgap.

Simulation Techniques

The mathematical model used in ATLAS takes account of these trap levels in two specific areas:

(i) an additional total charge term Q is added to the RHS of Poisson's equation.

(ii) modifications are added to the SRH model taking account of all traps

The total charge Q is calculated from first principles to be

$$Q=q(nt+pt)$$

where

$$nt=\int gA(E)\, fA(E,n,p)\, dE$$

$$pt=\int gD(E)\, fD(E,n,p)\, dE$$

g(E) is the DOS profile and f(E, n, p) is the probability of occupation of a trap.

Now there are two different implementation approaches that can be used in ***ATLAS*** to evaluate equation (1) which may be termed the DISCRETE and CONTINUOUS approaches.

The DISCRETE approach approximates the device physics in two ways

(i) the probability of occupation f(E,n,p) in equation (1) is moved outside the integral. This allows an analytical formula for g(E) to be easily calculated.

(ii) the continuous DOS profile is split into a number of individual discrete trap states with varying density of states and capture cross sections values.

A typical trap statement could look like

```
TRAP E.LEVEL=0.4 ACCEPTOR DENSITY=2e17 \
    DEGEN=1  SIGN=2.8E-15 SIGP=2.8E-14
```

This statement is then repeated many times for different energy levels across the bandgap for both the donor and acceptor states.

Note: The density of states is now the integrated value derived from some analytical expression which must be performed by the user.

The CONTINUOUS approach allows a self-consistent implementation of the device physics represented through equation (1). In this approach

(i) the probability of occupation f(E,n,p) in equation (1) is kept inside the integral.

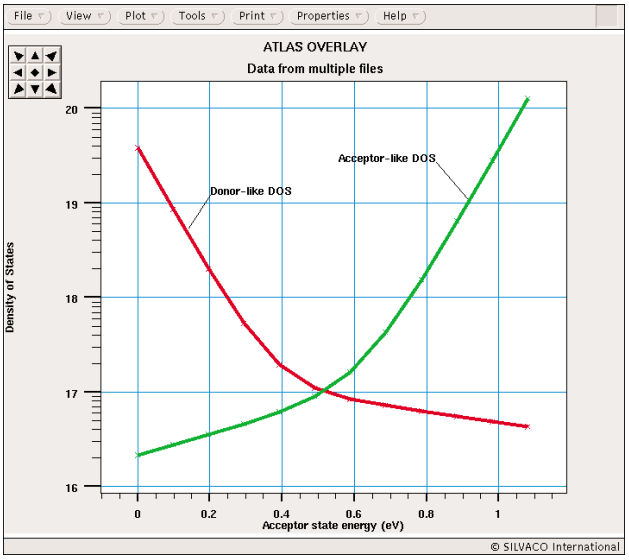

Figure 2 Density of States Profile for the Polysilicon TFT for both the donor and acceptor like traps..

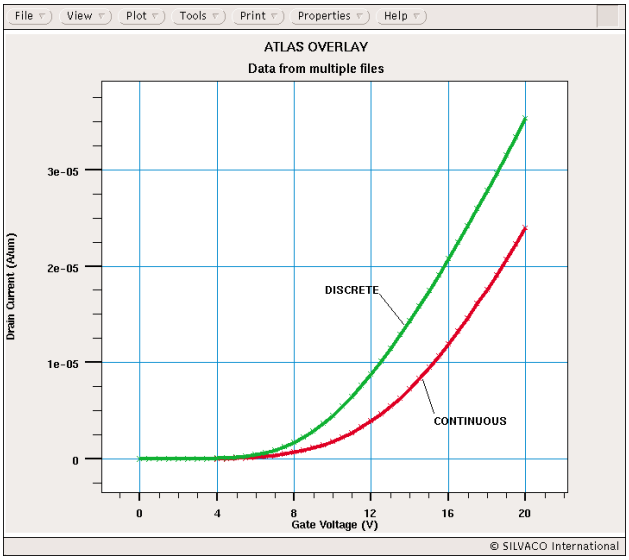

Figure 3 Id-Vg Characteristics of the TFT transistor showing the effect of the DISCRETE and CONTINUOUS models in the linear regime.

(ii) A numerical integration scheme is used to evaluate equation (1).

(iii) A C-interpreter function may be used to define the DOS profile.

A typical statement using the CONTINUOUS model would be of the form

```
defects CONTINUOUS f.tftdon=tft.lib \
        f.tftacc=tft.lib nta=0.0 ntd=0 nga=0 \
        ngd=0  wta=0.025 wtd=0.05 ega=0.4 \
        egd=0.4 wga=0.1 wgd=0.1sigtae=1.e-15 \
        sigtah=1.e-13 sigtde=1.e-13 \
        sigtdh=1.e-15 siggae=1.e-15 \
        siggah=1.e-13 siggde=1.e-13 \
        siggdh=1.e-15
```

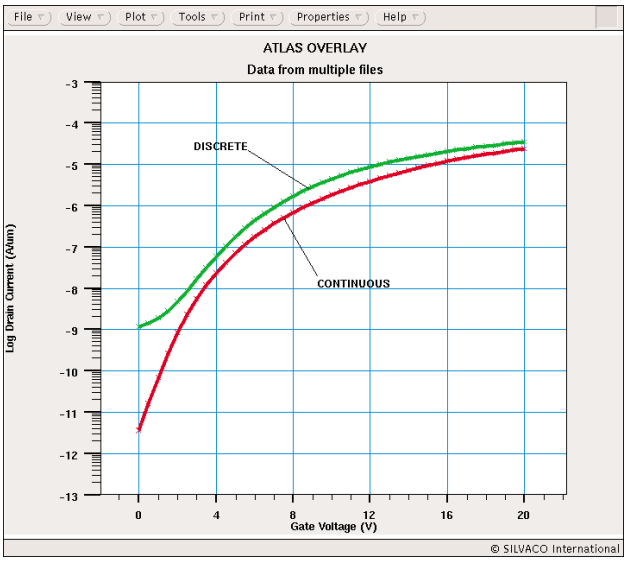

Figure 4 Log(Id)-Vg Characteristics of the TFT transistor showing the effect of the DISCRETE and CONTINUOUS models in the subthreshold regime.

Where "tft.lib" is a C-interpreter function containing the equations that describe the DOS profile for the donor and acceptor states.

Comparison of DISCRETE vs CONTINUOUS

To compare the two approaches a simple polysilicon transistor of gate length 10um was prepared in ATLAS. The structure of this three terminal device is shown in Figure 1. The literature has proposed many different DOS profiles for polysilicon TFT devices. The common thread has been that they are composed of two exponential functions [1] which may be written as

$$DOS = (Ntd^* \ e^{-E/E1}) + (Ndd^* \ e^{-E/E2})$$

In this work the resultant DOS profile is shown in Figure 2.

This device and the above DOS profile was simulated in ***ATLAS*** using both the DISCRETE and CONTINUOUS methods. The DISCRETE method used 12 individual trap levels to define the DOS profile. Figures 3 and 4 show the resultant Id-Vg and log(Id)-Vg characteristics

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Number of Trap Levels	CPU Time (sec)
6	206
12	260
24	453
124	1375

Table 1: CPU Time for Simulation to Complete Id/Vgs as a function of number of discrete trap levels.

Circuit Performance Analysis of Multiple *ATHENA* Transistors Using *MixedMode*

Introduction

In a previous issue of *Simulation Standard* for Process and Device Engineers[1] the simulation of a three stage CMOS ring oscillator using ***ATLAS/MixedMode*** was introduced. The MOSFETs used in the ***MixedMode*** simulation were created using analytical doping profiles specified within ***ATLAS***. This article is intended to investigate some of the effects of process variation on ring oscillator performance. Thus, the individual devices in the ring oscillator circuit are created usingthe two-dimensional process simulation program, ***ATHENA***.

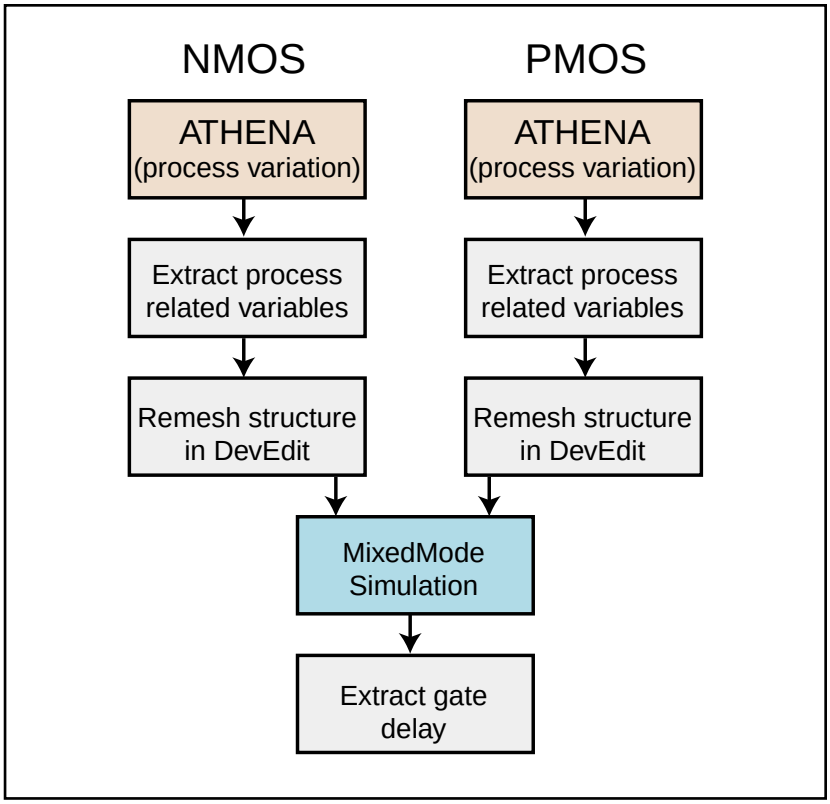

Figure 1. Simulation Methodology for multiple devices in ***MixedMode***.

Simulation Methodology

Figure 1 pictorially presents the simulation methodology used in this work. NMOS and PMOS devices were separately created in ***ATHENA***, where process conditions were specified (e.g., oxidation times and temperatures, etc.) and related process information was extracted (e.g., gate oxide thicknesses). The resulting NMOS and PMOS device structures were remeshed using ***DevEdit*** to concentrate the mesh in the inversion region and in regions where the doping concentration varied spatially. This structure remeshing provided a reduced node count for each device and a sufficient mesh for device simulation. The ring oscillator circuit (shown in Figure 2) was defined as it was in Part I [1], and the NMOS and PMOS transistors from the process simulation were used for each inverter in the circuit. As in Part I a piecewise linear waveform is applied to the supply voltage, causing the circuit to begin oscillating. Transient analysis is carried out for 500 picoseconds, and the gate delay is extracted from the voltage versus time waveforms according to equation 1 in Part I. The simulation scheme is automated using the ***VWF Automation Tools.***

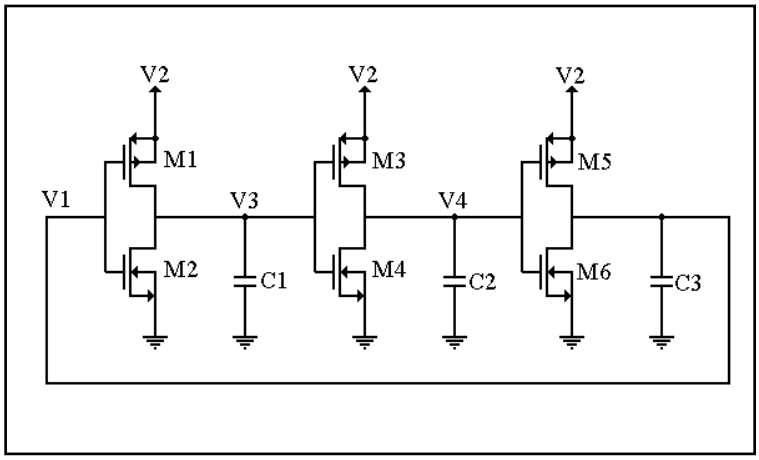

Figure 2. Schematic Diagram of Three Stage CMOS Ring Oscillator Used in MixedMode Simulations.

Simulation Results

Process variations were specified using a design of experiments created with the ***VWF Automation Tools***.. The process variables considered in this design of experiments were threshold voltage implant dose (Dose), gate oxidation temperature (T_{gate}). The numerical range of values considered in the experimental design are summarized in Table 1.

Using the process variations considered, a set of two-dimensional NMOS and PMOS

Process Variable	Range
Threshold Voltage Implant Dose (Dose)	$5x10^{12}$ - $9x10^{12}$ cm^{-2}
Gate Oxidation Temperature (T_{gate})	850 - 925 °C

Table 1. Process Variables and Ranges the experimental design

cross-sectional structures results. A representative structure for the NMOS device created with ***ATHENA*** is shown in Figure 3 (Dose = $5x10^{12}$ cm^{-2}, T_{gate} = 850 °C).

In Figure 4 the resulting transient voltage waveforms for two different gate oxidation temperatures are overlaid. The smaller period and thus gate delay for the lower oxidation temperature and thus thinner oxide thickness is evident when comparing the two waveforms.

Using the regression capability in the ***VWF Automation Tools***, a model describing the gate delay as a function of the process variables is created. This Response Surface Model (RSM) is shown as a contour plot in Figure 5.

Summary

Three stage ring oscillator simulations in ***ATLAS/MixedMode*** using ***ATHENA*** to define the NMOS and PMOS devices was demonstrated. ***DevEdit*** was used to remesh the device structure prior to transient ***MixedMode*** analysis. The gate delay time as a function of threshold voltage and gate oxidation was extracted from the transient ***MixedMode*** simulations. ***ATLAS/MixedMode***, ***ATHENA***, and the ***VWF Automation Tools*** can also be used to determine the dependence of the gate delay time on other process variables, and more sohpisticated response surface models can be realized.

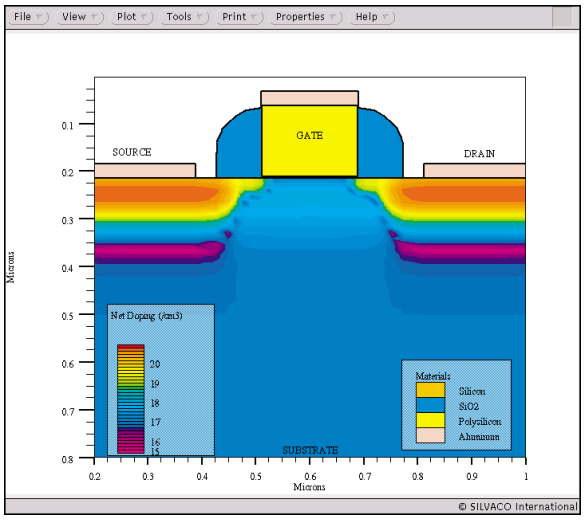

Figure 3. Two-dimensional Cross Section of NMOS Device Created with ***ATHENA*** (Dose = $5x10^{12}$ cm^{2}, T_{gate} = 850°C)

References

[1] "The Simulation Standard," pp. 3-4, May 1998.

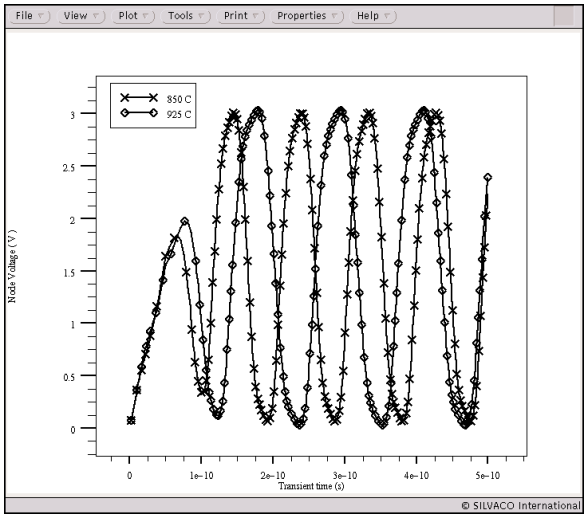

Figure 4: Transient Voltage on node 1 for 850 and 925 °C Gate Oxidation Temperature (Dose = $5x10^{12}$ cm^{-2}).

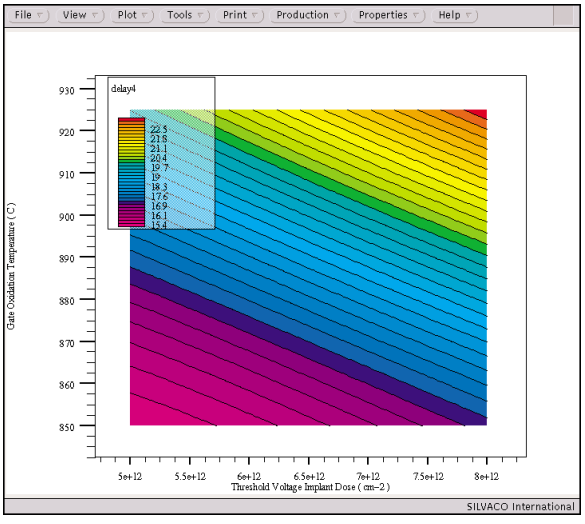

Figure 5: Contour plot of Gate Delay Versus Gate Oxidation Temperature and Threshold Voltage Implant Dose.

Calendar of Events

May

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2 ECS-SOI - Seattle, WA
3 ECS-SOI - Seattle, WA
4 ECS-SOI - Seattle, WA
5 ECS-SOI - Seattle, WA
6 ECS-SOI - Seattle, WA
7 ECS-SOI - Seattle, WA
8
9 Int'l Symposium on Plasma Process-Induced Damage - Monterey, CA
10 Int'l Symposium on Plasma Process-Induced Damage - Monterey, CA
11 Int'l Symposium on Plasma Process-Induced Damage - Monterey, CA
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16 CICC - San Diego, CA
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18 CICC - San Diego, CA
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24 IITC '99- Burlingame, CA
25 IITC '99- Burlingame, CA
26 IITC '99- Burlingame, CA Int'l Symp. On Power Semiconductor Devices and IC's - Toronto, Canada
27 Int'l Symp. On Power Semiconductor Devices and IC's - Toronto, Canada
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Bulletin Board

See Silvaco at DAC '99 Booth #514!

A large number of Silvaco new line engineers will be on hand at our booth for DAC '99 - New Orleans, LA from June 21-23. Stop by and get a demonstration in the latest TCAD Driven CAD. Highlights include:

- ***Expert*** and ***Savage*** - NT design system.
- ***Scholar*** - NT schematic editor
- ***Guardian*** - hierachical LVS
- ***Maverick*** - hierachical post-layout extractor
- parallel ***SmartSpice*** for UNIX and NT
- ***EXACT*** - technology driven interconnect parasitic extraction

CLEVER and EXACT 1999 Release available!

The latest release of ***DISCOVERY*** framework products for technology driven interconnect parasitic extraction will begin shipping in June. This release comes on CDROM with new advanced examples highlighting low-k processing. Shipping with the CDROM are completely revised manuals for both ***EXACT*** and ***CLEVER***.

Paper on CLEVER calibration presented at IITC '99!

The paper "New Interconnect Capacitance Characterization Method for Multi-Level Metal CMOS Processes" by Benoit Froment (ST) and Eric Guichard (Silvaco) et al was presented at the International Interconnect Technology Conference in Burlingame, CA on May 24-26. This work highlights a measurement technique and comparative ***CLEVER*** simulations of deep sub-micron interconnect parasitics.

If you would like more information or to register for one of our our workshops, please check our web site at ***http://www.silvaco.com***

Hints, Tips and Solutions

William French, Applications and Support Manager

Q: Which implant and diffusion models should be used for simulating MOS channel profiles in *ATHENA*?

Previous articles in the Simulation Standard have highlighted the diffusion models required for accurate simulation of shallow source / drain junction formation[1] and Reverse Short Channel Effect (RSCE)[2][3]. However for complete simulation of MOS short channel behavior it is necessary to consider the diffusion of the channel implants before the source / drain processing.

The NMOS channel process typically consists of a low energy boron or BF_2 implant to adjust the threshold voltage. This is often combined with a deeper implant for punch through protection. These implants are followed by the diffusion cycle used to form the gate oxide. Consideration of oxidation enhanced diffusion and dopant loss into the growing gate oxide is important.

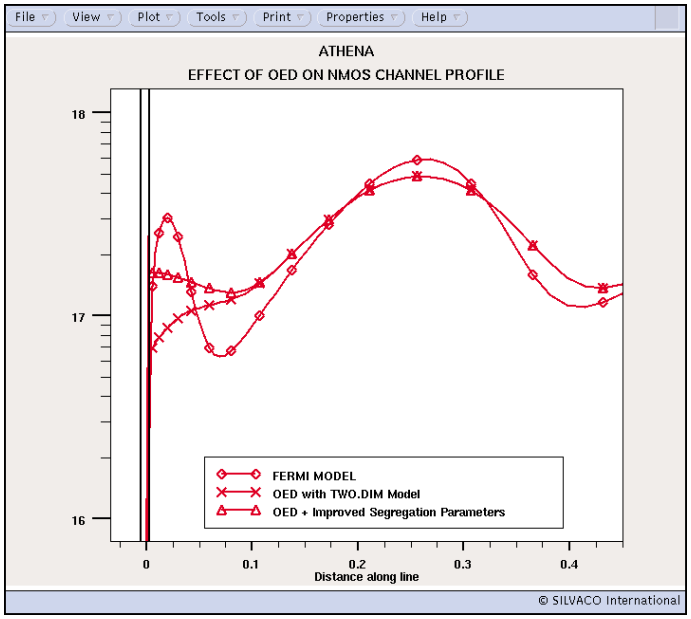

Figure 1. Comparison of FERMI and TWO.DIM models for NMOS channel implants and 8nm gate oxidation.

Firstly the as-implanted profiles should be simulated as accurately as possible. The default analytical SVDP implant models are accurate for boron implants of 5-80keV through native oxide or from 15-80keV through a thin screen oxide. For lower or higher energies it is recommended to use the BCA implant model. The results of the BCA simulation can be compared to the results from SVDP models. In some cases the results are similar and the quicker SVDP model can be used.

For subsequent diffusion steps with oxidizing ambients the `TWO.DIM` model must be selected on the `METHOD` statement. The `FERMI` model is not appropriate for these process steps. The `TWO.DIM` model correctly accounts for the injection of point defects into the substrate during oxidation and their effect on the diffusion rate of boron. Figure 1 illustrates the extra diffusion from the `TWO.DIM` model. Only 8nm of oxide was grown in this example. It is important to realize that the OED effect is not confined to the surface. The point defects diffuse quickly in silicon and affect the punch through implant profile too.

In addition to diffusion the channel implant has a dose loss by segregation into the gate oxide. This model is always enabled by default. Tuning the model is important though and Figure 1 shows that the effect of the segregation coefficient values can be down to a depth of 0.1µm.

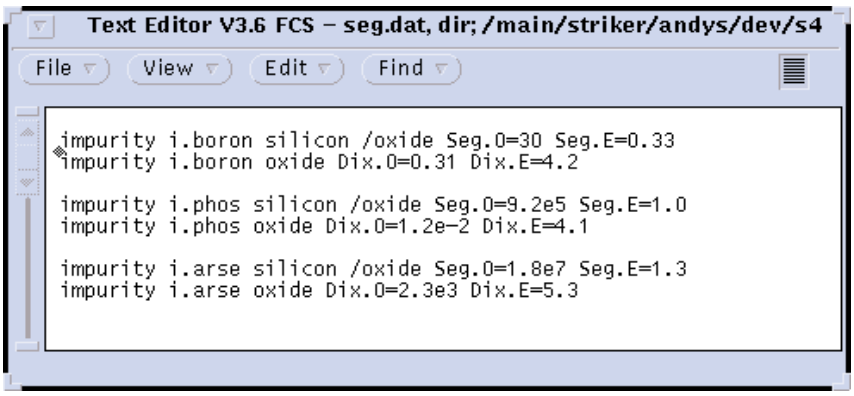

Figure 2. Temperature dependent segregation coefficients and oxide diffusion parameters for ***ATHENA***.

Modeling segregation accurately requires a fine grid both at the silicon surface and in the oxide. The GRID.OX parameter can be used to set the grid spacing in thermally grown oxides. The fine oxide grid is required since the diffusion of the dopant in oxide away from the interface can be important. Figure 2 shows a set of parameters for both segregation coefficients and diffusion in oxides from [4]. The dataset in this work was evaluated on oxides down to 3.5nm thick. Experience has shown that this parameter set has provided a more realistic starting point for tuning.

The channel profile obtained using these models will be valid for large channel devices and gate CV test structures. At short channel lengths the effect of defects from the source / drain areas will alter the doping profile causing RSCE. To verify this long channel profile users can use EXTRACT to determine the threshold voltage and the CV curve from a 1D simulation or a slice from a 2D simulation before the source drain diffusion. When tuning MOS channel profiles using threshold voltage it is important to extract the threshold voltage vs. back bias data and to fit the slope of this data. Fitting the slope is more important than actual threshold value since this is affected linearly by gate work function and oxide charge.

References

[1] Hints, Tips and Solutions, Simulation Standard, February 1995

[2] Hints, Tips and Solutions, Simulation Standard, December 1995

[3] "Calibrating RSCE", Simulation Standard, May 1998

[4] "Diffusion of As, P and B from Doped Polysilicon through Thin SiO2 Films into Si substrates", Matsuura et al., J. Electrochem. Soc. November 1991.

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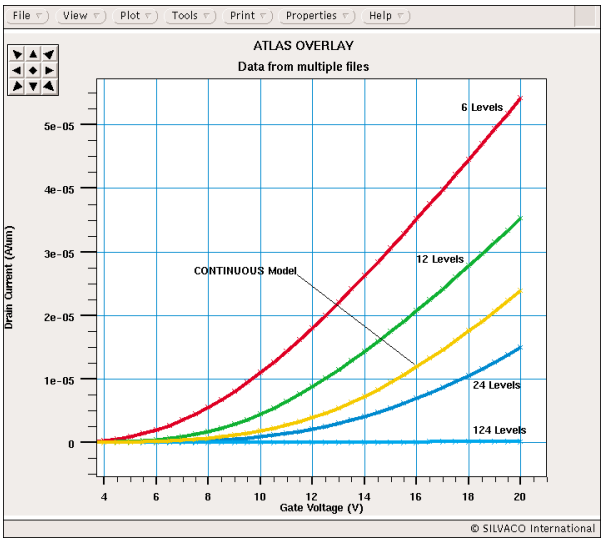


Figure 5. The number of trap levels in the DISCRETE model is shown to significantly influence the Id-Vg result. The CONTINOUS model does not have this this drawback.

obtained for the two cases. It is clear that the approximations in-built within the DISCRETE model cause significant loss of accuracy. Only the self-consistent, physically correct CONTINUOUS model will successfully model the physics of polysilicon TFT devices.

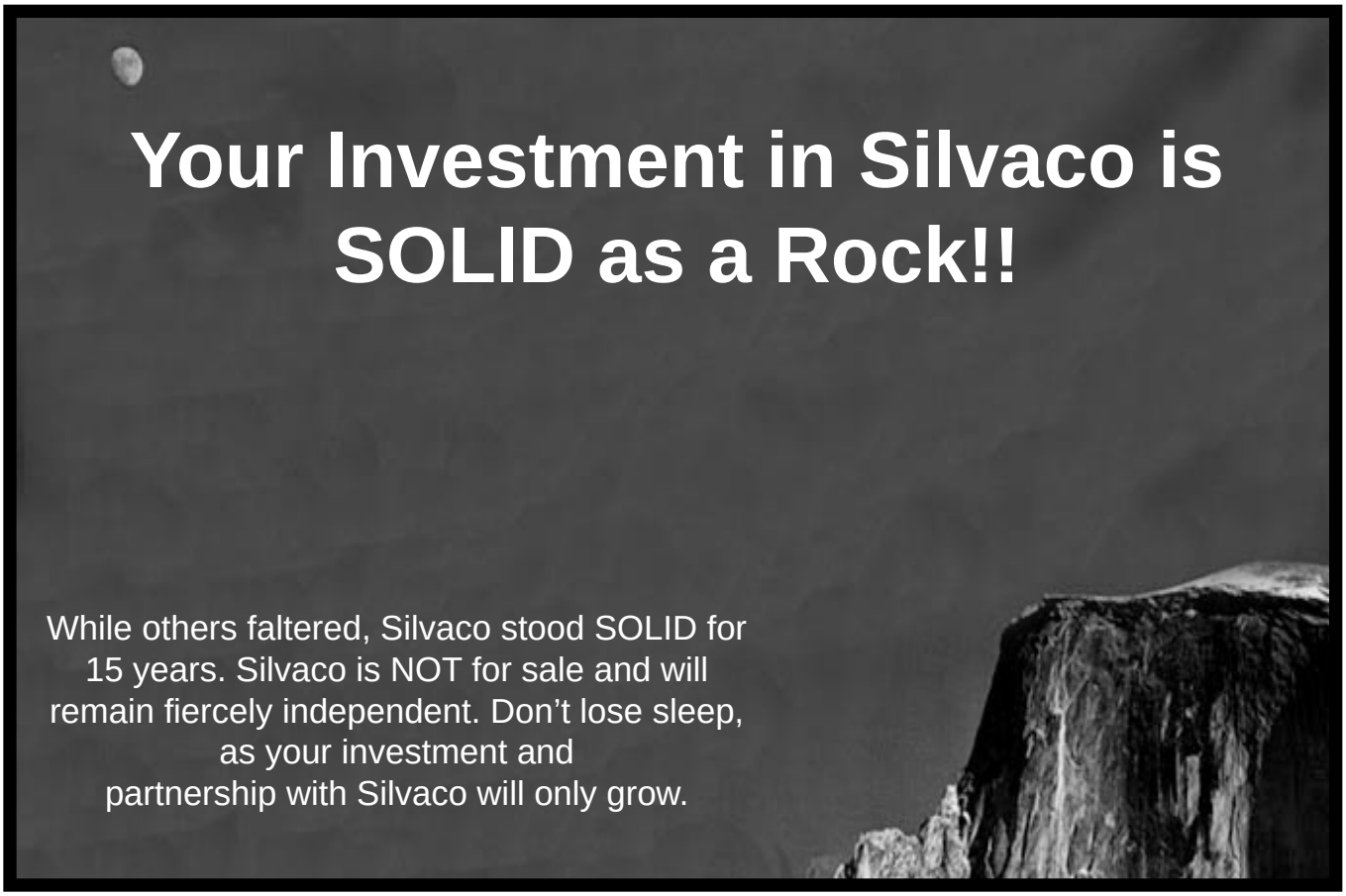
In addition the DISCRETE method requires the user to manually input a number of discrete levels into the simulator. There is no way, other than through trial and error, to know how many discrete trap levels are necessary to include. Varying the number of trap levels used significantly alters the results. Figure 5 shows the effect on the Id-Vg characteristic of increasing the number of trap levels from 6 to 124. Figure 5 shows the increasing cpu time that is then required when these levels are increased.

Conclusions

To maintain mathematical consistency in the TFT model it is necessary to model a CONTINUOUS profile of the DOS. It has been shown that the DISCRETE approach is inaccurate for a low number of trap levels and is cpu time sensitive to the number of trap levels. With the CONTINUOUS TFT model now implemented into ***ATLAS*** a self consistent scheme for modeling poly-silicon TFT transistors is now available. This scheme has the additional bonus of simplicity for the user, as it is not now necessary to define an integrated DOS profile or to discover how many discrete trap levels are necessary to maintain accuracy.

Reference

[1] G.A.Armstrong et al, "Modeling of Laser-Annealed Polysilicon TFT Characteristics", IEEE Elect. Dev. Lett., Vol. 18, No. 7, July 1997, pp. 315-318.



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