Circuit Performance Analysis of Multiple *ATHENA* Transistors Using *MixedMode*

Introduction

In a previous issue of *Simulation Standard* for Process and Device Engineers[1] the simulation of a three stage CMOS ring oscillator using ***ATLAS/MixedMode*** was introduced. The MOSFETs used in the ***MixedMode*** simulation were created using analytical doping profiles specified within ***ATLAS***. This article is intended to investigate some of the effects of process variation on ring oscillator performance. Thus, the individual devices in the ring oscillator circuit are created usingthe two-dimensional process simulation program, ***ATHENA***.

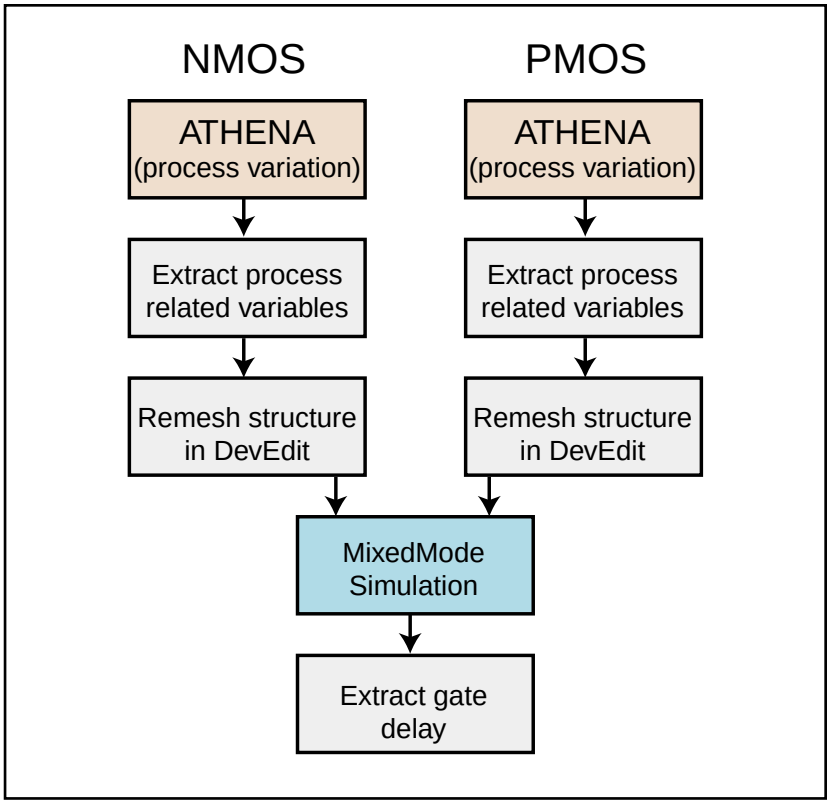

Figure 1. Simulation Methodology for multiple devices in ***MixedMode***.

Simulation Methodology

Figure 1 pictorially presents the simulation methodology used in this work. NMOS and PMOS devices were separately created in ***ATHENA***, where process conditions were specified (e.g., oxidation times and temperatures, etc.) and related process information was extracted (e.g., gate oxide thicknesses). The resulting NMOS and PMOS device structures were remeshed using ***DevEdit*** to concentrate the mesh in the inversion region and in regions where the doping concentration varied spatially. This structure remeshing provided a reduced node count for each device and a sufficient mesh for device simulation. The ring oscillator circuit (shown in Figure 2) was defined as it was in Part I [1], and the NMOS and PMOS transistors from the process simulation were used for each inverter in the circuit. As in Part I a piecewise linear waveform is applied to the supply voltage, causing the circuit to begin oscillating. Transient analysis is carried out for 500 picoseconds, and the gate delay is extracted from the voltage versus time waveforms according to equation 1 in Part I. The simulation scheme is automated using the ***VWF Automation Tools.***

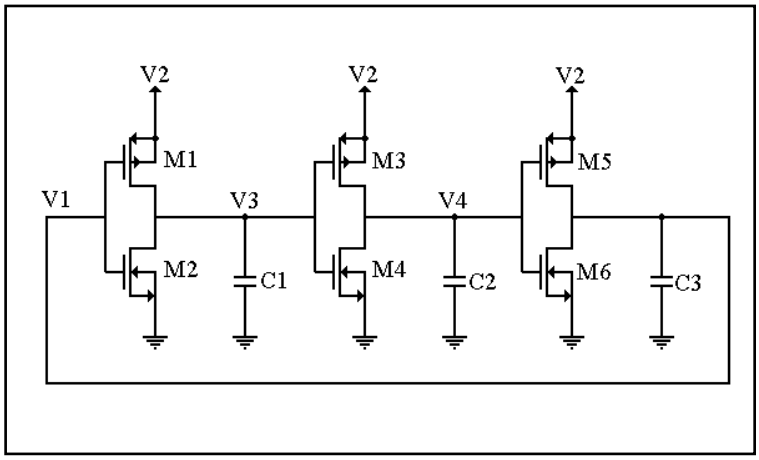

Figure 2. Schematic Diagram of Three Stage CMOS Ring Oscillator Used in MixedMode Simulations.

Simulation Results

Process variations were specified using a design of experiments created with the ***VWF Automation Tools***.. The process variables considered in this design of experiments were threshold voltage implant dose (Dose), gate oxidation temperature (T_{gate}). The numerical range of values considered in the experimental design are summarized in Table 1.

Using the process variations considered, a set of two-dimensional NMOS and PMOS

Process Variable	Range
Threshold Voltage Implant Dose (Dose)	$5x10^{12}$ - $9x10^{12}$ cm^{-2}
Gate Oxidation Temperature (T_{gate})	850 - 925 °C

Table 1. Process Variables and Ranges the experimental design

cross-sectional structures results. A representative structure for the NMOS device created with ***ATHENA*** is shown in Figure 3 (Dose = $5x10^{12}$ cm^{-2}, T_{gate} = 850 °C).

In Figure 4 the resulting transient voltage waveforms for two different gate oxidation temperatures are overlaid. The smaller period and thus gate delay for the lower oxidation temperature and thus thinner oxide thickness is evident when comparing the two waveforms.

Using the regression capability in the ***VWF Automation Tools***, a model describing the gate delay as a function of the process variables is created. This Response Surface Model (RSM) is shown as a contour plot in Figure 5.

Summary

Three stage ring oscillator simulations in ***ATLAS/MixedMode*** using ***ATHENA*** to define the NMOS and PMOS devices was demonstrated. ***DevEdit*** was used to remesh the device structure prior to transient ***MixedMode*** analysis. The gate delay time as a function of threshold voltage and gate oxidation was extracted from the transient ***MixedMode*** simulations. ***ATLAS/MixedMode***, ***ATHENA***, and the ***VWF Automation Tools*** can also be used to determine the dependence of the gate delay time on other process variables, and more sohpisticated response surface models can be realized.

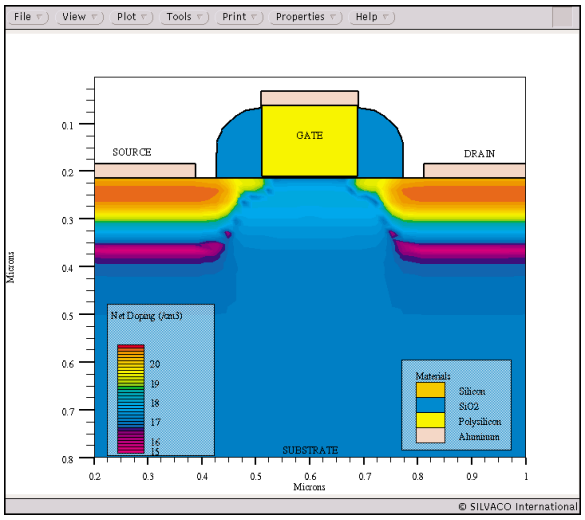

Figure 3. Two-dimensional Cross Section of NMOS Device Created with ***ATHENA*** (Dose = $5x10^{12}$ cm^{2}, T_{gate} = 850°C)

References

[1] "The Simulation Standard," pp. 3-4, May 1998.

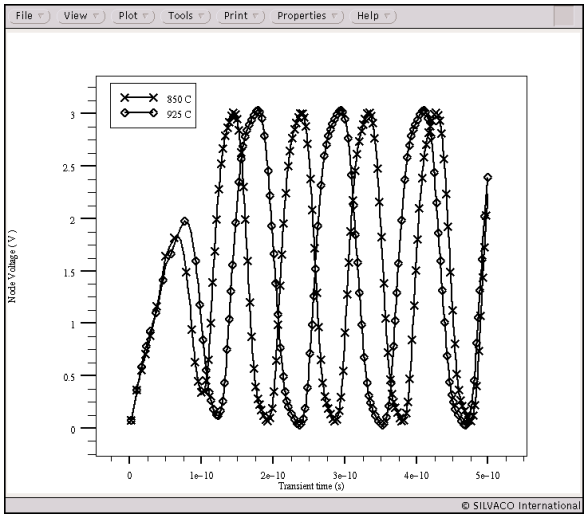

Figure 4: Transient Voltage on node 1 for 850 and 925 °C Gate Oxidation Temperature (Dose = $5x10^{12}$ cm^{-2}).

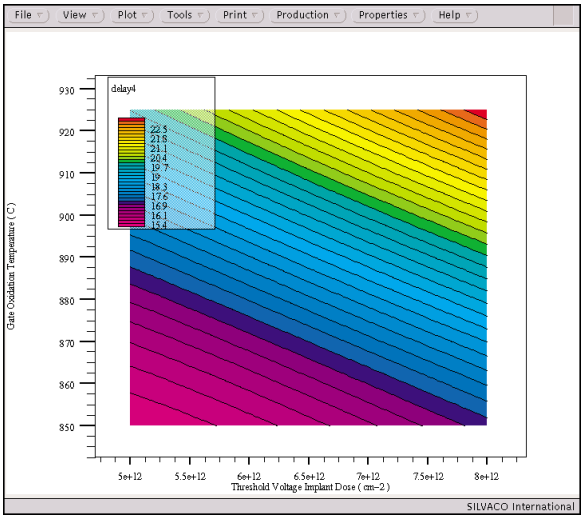

Figure 5: Contour plot of Gate Delay Versus Gate Oxidation Temperature and Threshold Voltage Implant Dose.