Continous Trap Model for Accurate Device Simulation of Polysilicon TFTs

System on a Panel Requirements

There has been a significant increase in the popularity of liquid crystal displays with control circuitry being placed on to the glass (system on a panel). This has been made possible by the technological improvements of thin-film-transistors (TFTs) manufactured on glass substrates. The sudden popularity is a result of the move away from the traditional use of amorphous silicon towards polycrystalline silicon. The increase in performance by this switch has allowed these TFTs to be applied to applications beyond pixel control transistors.

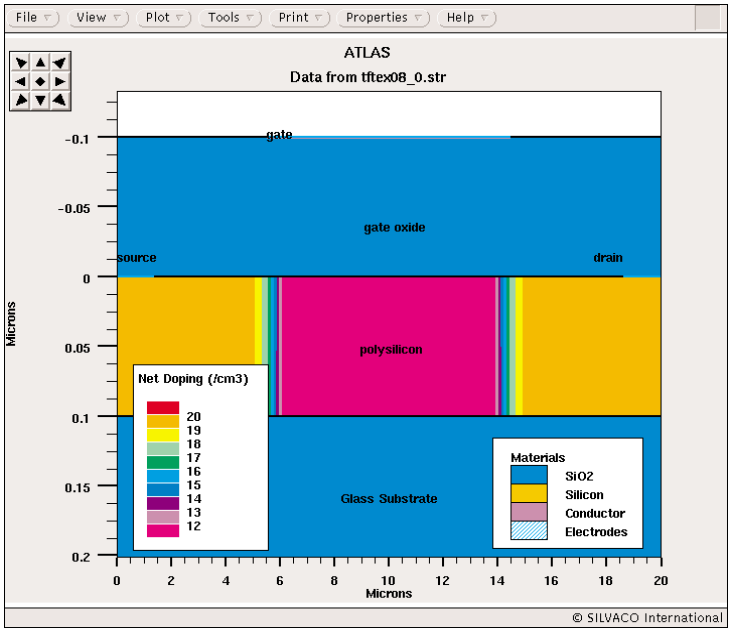

Figure 1. Geometry and doping profile of the Polysilicon TFT to be simulated.

In order to design circuits using TFTs it is fundamentally necessary to understand the physics involved in their operation. The best way of achieving this is through two-dimensional device simulation. Polysilicon consists of a number of grain and grain boundary regions. Improvements in processing have resulted in quite large, ~0.5um, well controlled grain regions. Within the grain boundaries there exists trapped charge which act as potential barriers. The effect of the trapped charge can then be modeled by defining the average band bending which is determined by the spatially averaged trapped charge density. By this means it is possible to calculate a continuous, volume averaged, density of states (DOS) profile across the band gap. This DOS profile is modeled using profiles of acceptor-like and donor-like traps distributed across the bandgap.

Simulation Techniques

The mathematical model used in ATLAS takes account of these trap levels in two specific areas:

(i) an additional total charge term Q is added to the RHS of Poisson's equation.

(ii) modifications are added to the SRH model taking account of all traps

The total charge Q is calculated from first principles to be

$$Q=q(nt+pt)$$

where

$$nt=\int gA(E)\, fA(E,n,p)\, dE$$

$$pt=\int gD(E)\, fD(E,n,p)\, dE$$

g(E) is the DOS profile and f(E, n, p) is the probability of occupation of a trap.

Now there are two different implementation approaches that can be used in ***ATLAS*** to evaluate equation (1) which may be termed the DISCRETE and CONTINUOUS approaches.

The DISCRETE approach approximates the device physics in two ways

(i) the probability of occupation f(E,n,p) in equation (1) is moved outside the integral. This allows an analytical formula for g(E) to be easily calculated.

(ii) the continuous DOS profile is split into a number of individual discrete trap states with varying density of states and capture cross sections values.

A typical trap statement could look like

```
TRAP E.LEVEL=0.4 ACCEPTOR DENSITY=2e17 \
    DEGEN=1  SIGN=2.8E-15 SIGP=2.8E-14
```

This statement is then repeated many times for different energy levels across the bandgap for both the donor and acceptor states.

Note: The density of states is now the integrated value derived from some analytical expression which must be performed by the user.

The CONTINUOUS approach allows a self-consistent implementation of the device physics represented through equation (1). In this approach

(i) the probability of occupation f(E,n,p) in equation (1) is kept inside the integral.

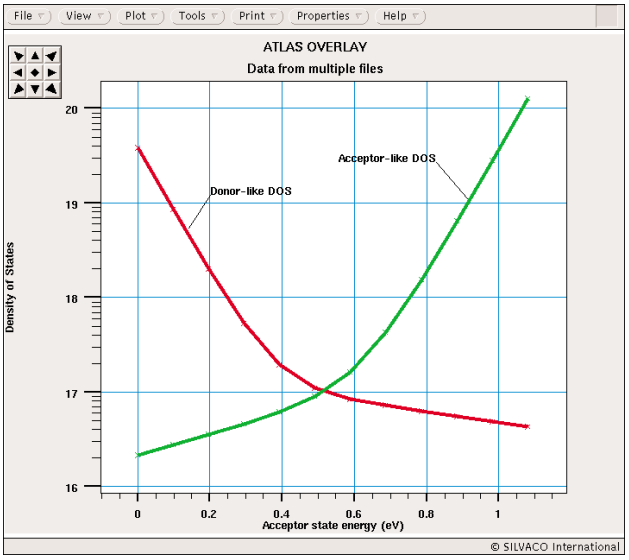

Figure 2 Density of States Profile for the Polysilicon TFT for both the donor and acceptor like traps..

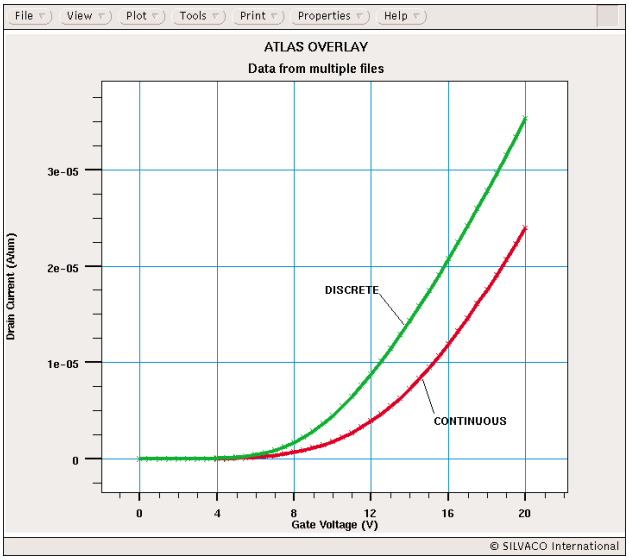

Figure 3 Id-Vg Characteristics of the TFT transistor showing the effect of the DISCRETE and CONTINUOUS models in the linear regime.

(ii) A numerical integration scheme is used to evaluate equation (1).

(iii) A C-interpreter function may be used to define the DOS profile.

A typical statement using the CONTINUOUS model would be of the form

```
defects CONTINUOUS f.tftdon=tft.lib \
        f.tftacc=tft.lib nta=0.0 ntd=0 nga=0 \
        ngd=0  wta=0.025 wtd=0.05 ega=0.4 \
        egd=0.4 wga=0.1 wgd=0.1sigtae=1.e-15 \
        sigtah=1.e-13 sigtde=1.e-13 \
        sigtdh=1.e-15 siggae=1.e-15 \
        siggah=1.e-13 siggde=1.e-13 \
        siggdh=1.e-15
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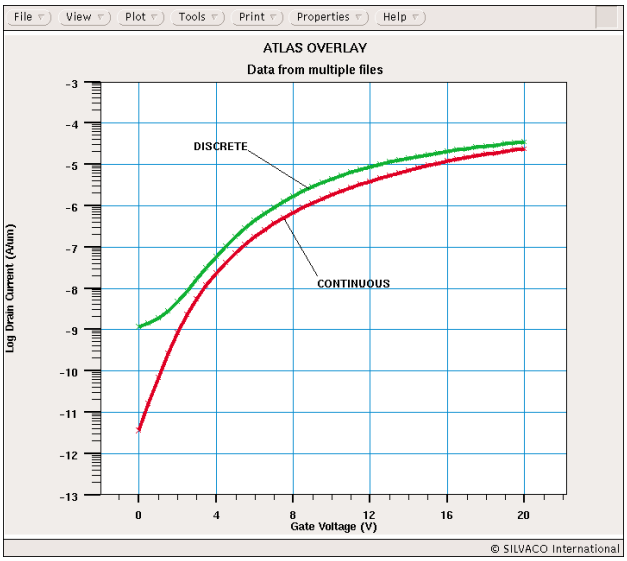

Figure 4 Log(Id)-Vg Characteristics of the TFT transistor showing the effect of the DISCRETE and CONTINUOUS models in the subthreshold regime.

Where "tft.lib" is a C-interpreter function containing the equations that describe the DOS profile for the donor and acceptor states.

Comparison of DISCRETE vs CONTINUOUS

To compare the two approaches a simple polysilicon transistor of gate length 10um was prepared in ATLAS. The structure of this three terminal device is shown in Figure 1. The literature has proposed many different DOS profiles for polysilicon TFT devices. The common thread has been that they are composed of two exponential functions [1] which may be written as

$$DOS = (Ntd^* \ e^{-E/E1}) + (Ndd^* \ e^{-E/E2})$$

In this work the resultant DOS profile is shown in Figure 2.

This device and the above DOS profile was simulated in ***ATLAS*** using both the DISCRETE and CONTINUOUS methods. The DISCRETE method used 12 individual trap levels to define the DOS profile. Figures 3 and 4 show the resultant Id-Vg and log(Id)-Vg characteristics

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Number of Trap Levels	CPU Time (sec)
6	206
12	260
24	453
124	1375

Table 1: CPU Time for Simulation to Complete Id/Vgs as a function of number of discrete trap levels.

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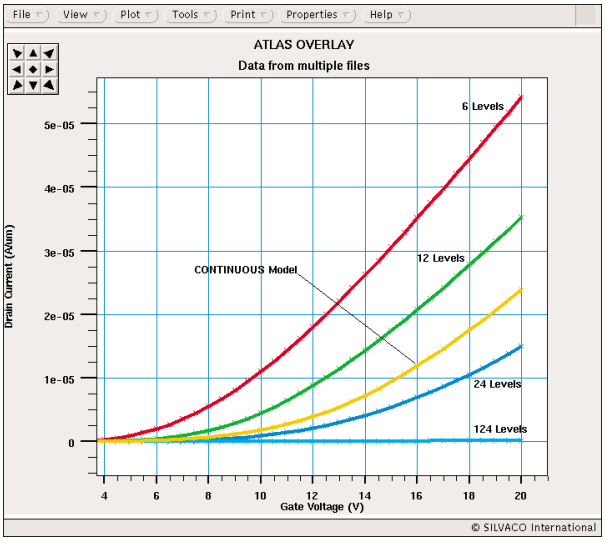

Figure 5. The number of trap levels in the DISCRETE model is shown to significantly influence the Id-Vg result. The CONTINOUS model does not have this this drawback.

obtained for the two cases. It is clear that the approximations in-built within the DISCRETE model cause significant loss of accuracy. Only the self-consistent, physically correct CONTINUOUS model will successfully model the physics of polysilicon TFT devices.

In addition the DISCRETE method requires the user to manually input a number of discrete levels into the simulator. There is no way, other than through trial and error, to know how many discrete trap levels are necessary to include. Varying the number of trap levels used significantly alters the results. Figure 5 shows the effect on the Id-Vg characteristic of increasing the number of trap levels from 6 to 124. Figure 5 shows the increasing cpu time that is then required when these levels are increased.

Conclusions

To maintain mathematical consistency in the TFT model it is necessary to model a CONTINUOUS profile of the DOS. It has been shown that the DISCRETE approach is inaccurate for a low number of trap levels and is cpu time sensitive to the number of trap levels. With the CONTINUOUS TFT model now implemented into ***ATLAS*** a self consistent scheme for modeling poly-silicon TFT transistors is now available. This scheme has the additional bonus of simplicity for the user, as it is not now necessary to define an integrated DOS profile or to discover how many discrete trap levels are necessary to maintain accuracy.

Reference

[1] G.A.Armstrong et al, "Modeling of Laser-Annealed Polysilicon TFT Characteristics", IEEE Elect. Dev. Lett., Vol. 18, No. 7, July 1997, pp. 315-318.