Simulation Standard

TCAD Driven CAD

A Journal for Circuit Simulation and SPICE Modeling Engineers

New SOI *UTMOST* Module

Introduction

Bulk CMOS is currently the dominant technology for VLSI integrated circuits but its scaling constraints pose ever greater as device geometries shrink. Thus, the search for a suitable replacement has begun, and Silicon-On-Insulator (SOI) technology seems to become the most attractive candidate for a suitable VLSI / CMOS technology.

The SOI technology differs significantly from the bulk technology due to the burried oxide. Because of this specific structure, SOI MOSFETs exhibit many anomalous static and dynamic effects which can be attributed to either the floating body or to self heating. Consequently, in addition to the usual Bulk MOSFET, several other characteristics must be observed to characterize correctly and accurately SOI devices. SOI utmost module has been improved accordingly to these criteria, and is presented in this article.

SOI Module specificities

Number of Terminals

SOI devices are commonly designed with 4 terminals : Drain, Gate, Source and BackGate terminals. It can also be designed with a fifth terminal in order to access the internal Body (equivalent to MOS Substrate terminal). Users can switch between 4 and 5 terminals devices through the "# of Terminals" button of the Common Control Screen.

The SMU Definition Screen will be so modified accordingly to the number of terminals selected. For example, in the HP4145 case and for 5 terminal devices, the BackGate terminal will be applied on the VS1 Unit. For the HP4156, the user will be able to choose between SMU5 (if he can use this SMU) or VS1.

The general syntax to define a SOI device in ***UTMOST***, is:

MXX ND NG NS NBG (NB) MNAME
(L=Lavlue) (W=Wvalue)

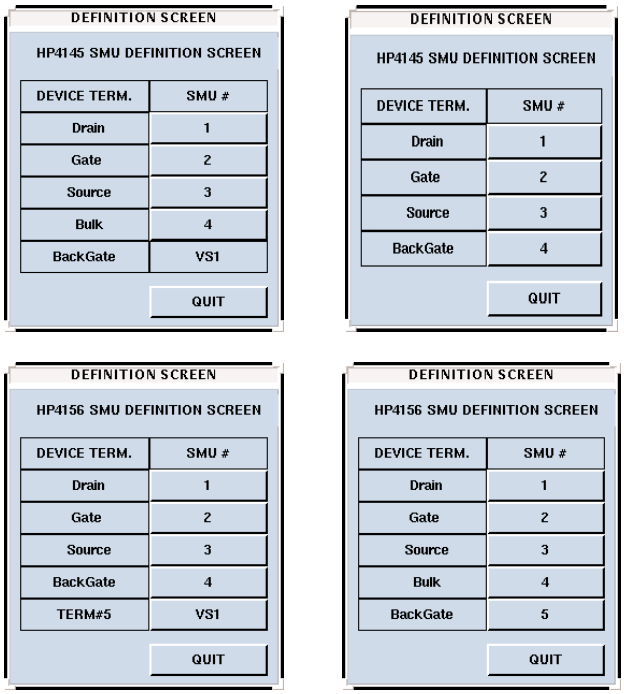

Figure 1. SMU Definition Screens for HP4145 and HP4156.

where ND is the Drain node, NG is the Gate node, NS is the Source node, NBG is the BackGate node, and NB is the optional Body node. This Body node should be present in case of body contacted devices. MNAME is the model name while L and W are respectively the length and width of the device.

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INSIDE

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Common Routines

ID/VD-VG Routine

This routine comes from the well known ID/VD-VG MOS routine, and has been adapted to the SOI Module allowing users to measure, simulate and optimize Output characteristics. Rubberband and modeling are also available. The drain voltage is swept over a defined voltage range for a set of VG values. BackGate (and Body if accessible) are kept to constant values.

The DC Measurement Screen variables are described below. The number of VG steps is defined in the Measurement Section field now available in both DC Measurement Screen and Routine Control Screen.

VDS_start	Starting value of the Drain voltage sweep range.
VDS_stop	Stop value of the Drain voltage range.
points	Number of sweep data points.
VGS_start	Starting value of Gate voltage.
VGS_stop	Step value of the Gate voltage.
VBG_or_Body	Constant voltage applied to BackGate (if Stepflag=0) or to Body-contact (if Stepflag=1).
V_constant	Constant voltage applied to Body-contact (if Stepflag=0) or to BackGate (if Stepflag=1); only used with 5 terminals.
compl_smu(A)	SMU current compliances.
wait	Wait time in microseconds, between measurements
Stepflag	BackGate-Body switch flag.

ID/VG-VB Routine

This routine also comes from the well know ID/VG-VB MOS routine. It is dedicated to the transcharacteristic analysis. Measurement, simulation, optimization, rubberband and modeling are available for this routine. The Gate voltage is swept over a defined range for a set of BackGate (or Body) values. In case of 5 terminals Body (or BackGate) is kept to a constant value. Drain is kept to a constant value too.

The DC Measurement Screen variables are described below. The number of VBG (or VBody) steps is defined in the Measurement Section field now available in both DC Measurement Screen and Routine Control Screen.

VGS_start	Starting value of the Gate voltage sweep range.
VGS_stop	Stop value of the Gate voltage range.
points	Number of sweep data points.
VD	Constant Drain voltage.
V_start	Starting value for the stepped voltage (Body if Stepflag=1, BackGate if Stepflag=0).
V_step	Step value for the stepped voltage Body if Stepflag=1, BackGate if Stepflag=0).
V_constant	Constant voltage applied to BackGate (if Stepflag=1)or to Body (if Stepflag=0 voltage ; only used with 5 terminals.
compl_smu(A)	SMU current compliances.
wait	Wait time in microseconds, between measurements.
Stepflag	Body voltage is stepped if 1, else BackGate voltage is stepped; only active with 5 terminals.

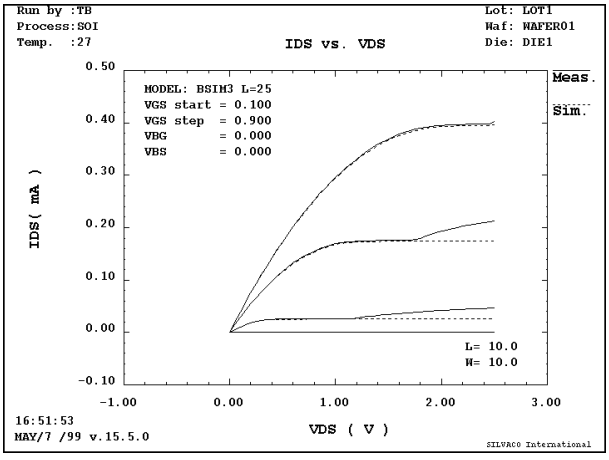

Figure 2. Typical ID/VD-VG Measured Data Set. SOI characteristic in continuous line, and SOI with Body-Contact in dashed line.

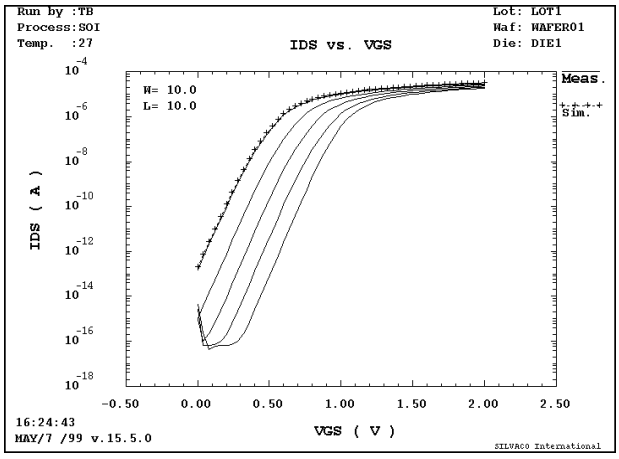

Figure 3. Typical SOI ID(VG) characteristic for several VBackGate (4 terminals) with markers and dashed lines. Usual ID/VG characteristic for several VBody (5 terminals, stepflag=1) in continuous lines.

ALL_DC Routine

Identical to the MOS Module, the ALL_DC routine is a multi-geometry and multi-characteristic routine. This routine will allow the user to display both ID/VG-VB and ID/VD-VG curves for several devices on the same plot. This is a powerful routine, which will be strongly recommended for multiple optimizations. This routine is available for measurement, simulation, optimization, rubberband and modeling features.

The DC Measurement Screen variables are described below. The number of VG and VBG (or VBody) steps are defined in the Measurement Section field now available in both DC Measurement Screen and Routine Control Screen.

VD_start_vd	Starting value for the Drain voltage sweep (ID/VD curves).
VD_stop_vd	Stop value for the Drain voltage range (ID/VD curves).
VG_start_vd	Starting value of the Gate voltage step (ID/VD curves).
VG_step_vd	Step value for the Gate voltage (ID/VD curves).
V_start_vd	Starting value of the BackGate (or Body) voltage second step (ID/VD curves).
V_step_vd	Step value for the BackGate (or Body) voltage second step (ID/VD curves).
V_points_vd	Number of BackGate (or Body) step points (ID/VD curves).
V_const_vd	Constant Body (or BackGate) voltage value ; only used with 5 terminals (ID/VD curves).
VG_start_vg	Starting value for the Gate voltage sweep (ID/VG curves).
VG_stop_vg	Stop value for the Gate voltage range (ID/VG curves).
VD_vg	Constant Drain voltage value (ID/VG curve).
V_start_vg	Starting value for the BackGate (or Body) voltage step (ID/VG curves).

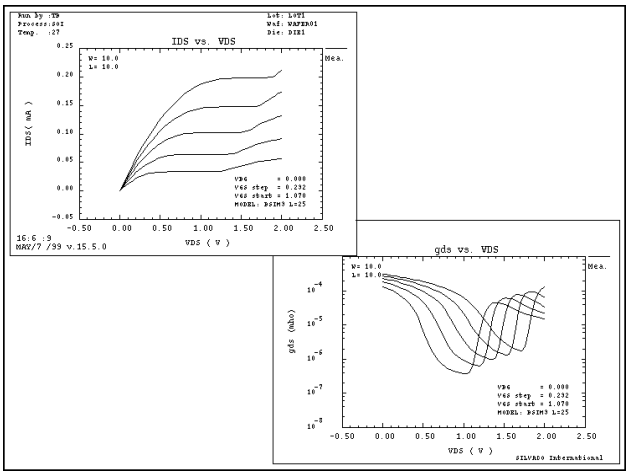

Figure 4.Typical ALL_DC plot, with ID/VD and gds targets for a partially depleted SOI device.

V_step_vg	Step value for the BackGate (or Body) voltage step (ID/VG curves).
V_const_vg	Constant Body (or BackGate) voltage value ; only used with 5 terminals (ID/VG curves).
points	Number of sweep data points.
ALL0,VD1,VG2	If 0, both ID/VD and ID/VG curves are measured. If 1, only ID/VD curves are measured. If 2, only ID/VG curves are measured.
compl_smu(A)	SMU current compliances.
wait	Wait time in microseconds, between measurements.
Stepflag	If 0, V_start,step,.._vd(vg) are applied on BackGate, and V_const_vd(vg) are applied on Body. If 1, V_start,step,.._vd(vg) are applied on Body, and V_const_vd(vg) are applied on BackGate. Only used with 5 terminals.

To avoid confusion between BackGate and Body value, varaible definitions can be given as in Table 1.

Measurement variables	**4 terminals**	**5 terminals**	
		stepflag=0	**stepflag=1**
V_start_vd, V_step_vd, V_points_vd	VBackGate @ID/VD	VBackGate @ID/VD	VExt Body @ID/VD
V_const_vd	Not Used	VExt Body @ID/VD	VBackGate @ID/VD
V_start_vg, V_stop_vg	VBackGate @ID/VG	VBackGate @ID/VG	VExt Body @ID/VG
V_const_vg	Not Used	VExt Body @ID/VG	VBackGate @ID/VG

Table 1.

BSIM3_MG routine

BSIM3_MG routine derived from the MOS module and has been adapted for the SOI module. As for the MOS module, this routine will manage four characteristics: ID/VD-VG with 0V on BackGate (or Body), ID/VG-VB for low VD, ID/VD-VG for high BackGate (or Body) bias, and ID/VG-VB for high VD. If this routine is used with 5 terminals and stepflag=1, curves will be obtained as for a MOS device. All BSIM3 model parameters, as can be done in the MOS module, will be extracted

The DC Measurement Screen is described below. The number of VG steps is given through the #_of_vgsteps variable, and the number of VBG (or VBody) steps is given through the #_of_vbsteps variable.

VGS_start_vg — Starting value for the Gate voltage sweep (ID/VG curves).

VGS_stop_vg — Stop value for the Gate voltage range (ID/VG curves).

VDS_low_vg — Low constant Drain voltage for the linear region (ID/VG curves).

VDS_high_vg — High constant Drain voltage for the saturation region (ID/VG curves).

VDS_start_vd — Starting value for the Drain voltage sweep (ID/VD curves).

VDS_stop_vd — Stop value for the Drain voltage range (ID/VD curves).

VGS_strt1_vd — Starting value of the Gate voltage step (ID/VD curves with VBG(or VBody)=0V) ; value calculated from extracted threshold voltage and VGS_strt_off.

VGS_strt2_vd — Starting value of the Gate voltage step (ID/VD curves with VBG(or VBody)=V_stop_vd) ; value calculated from extracted threshold voltage and VGS_strt_off.

VGS_strt_off — Offset voltage used to determine VGS_strt1_vd and VGS_strt2_vd values.

V_stop_vd — Maximum BackGate (or Body) voltage (ID/VD curves).

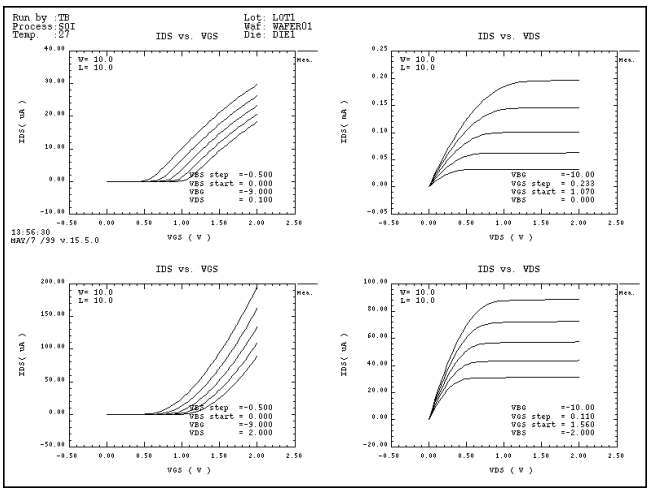

Figure 5. Example of BSIM3_MG measurement for a long and large device. Case 5 terminals, and Stepflag=1.

V_const_vd — Constant Body (or BackGate) voltage (ID/VD curves) ; only used with 5 terminals.

compl_smu(A) — SMU current compliances

points — Number of sweep data points.

V_stop_vg — Maximum BackGate (or Body) step voltage (ID/VG curves).

V_const_vg — Constant Body (or BackGate) voltage (ID/VG curves).

wait — Wait time in microseconds, between measurements.

#_of_vgsteps — Number of VG steps (ID/VD curves).

#_of_vbsteps — Number of VBG (or VBody) steps (ID/VG curves).

Stepflag — If 0, V_stop_vd(vg) are applied on Backgate ; V_const_vd(vg) are applied on Body. If 1, V_stop_vd(vg) are applied on Body ; V_const_vd(vg) are applied on BackGate. Only used with 5 terminals.

To avoid confusion between BackGate and Body value, varaible definitions can be given as in Table 2.

Measurement Variables	4 terminals	5 terminals	
		stepflag=0	stepflag=1
V_stop_vd	VBackGate @ID/VD	VBackGate @ID/VD	VExt Body @ID/VD
V_const_vd	Not Used	VExt Body @ID/VD	VBackGate @ID/VD
V_stop_vg	VBackGate @ID/VG	VBackGate @ID/VG	VExt Body @ID/VG
V_const_vg	Not Used	VExt Body @ID/VG	VBackGate @ID/VG
#_of_vgsteps	VGate Steps @ ID/VD		
#_of_vbsteps	VBackGate Steps @ ID/VG	VBackGate Steps @ ID/VG	VExt Body Steps @ ID/VG

Table 2.

The extraction part of this routine is derived from the MOS module, and allows the user to extract the whole MOS BSIM3 model parameters of the BSIM3SOI model.

Currently, this routine is only able to extract low VD model parameters.

AL_IDVGD Routine

This last routine also comes from the MOS module. This is a new multi-geometry routine, which allows users to measure the drain current over a defined gate sweep voltage for several drain voltages. A second step can be applied on the BackGate with 4 terminal devices, and on the Body with 5 terminal devices. This routine allows the measurement, simulation, optimization, rubberband and modeling features.

The DC Measurement Screen is described below. The number of VD steps is defined in the Measurement Section field.

VGS_start	Starting value of the Gate voltage sweep range.
VGS_stop	Stop value of the Gate voltage range.
points	Number of sweep data points.
VD_start	Starting value of the Drain step voltage.
VD_step	Step value of the Drain voltage.
VB_start	Starting Backgate voltage value in case of 4 terminals. Starting Body voltage value in case of 5 terminals.
VB_step	Step BackGate voltage value in case of 4 terminals. Step Body voltage value in case of 5 terminals.
VB_points	Defines the number of BackGate (or Body) bias points.
VB5_cst	BackGate constant voltage ; only used with 5 terminals.
VS	Constant Source voltage.
complsdb(A)	SMU current compliances.
wait	Wait time in microseconds, between measurements.
IDS_low_cut	Drain low current limit to filter noisy data points.

New Specific Routines

For the five next routines, as we will measure or bias the Body, 5 terminals devices are requested. So, 5 should set for the “of terminals” button. Otherwise, a message will appear in the main ***UTMOST*** window.

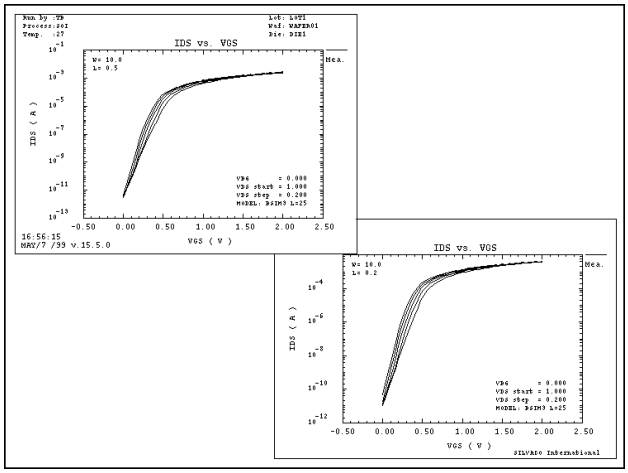

Figure 6. Typical ID/VG-VD curves for partially depleted SOI devices.

IB/VG_MG Routine

This routine stems from the well known ALL_ISUB MOS routine, and is dedicated to characterize the Impact Ionisation current. As for ALL_ISUB, it is a multi-geometry routine. Measurement, simulation, optimization, rubberband and modeling are available. Internal Body current is measured over a defined gate voltage sweep range, for several drain constant steps, and eventually for various second Body values. During all measurements, source and backgate are kept to constant values.

The DC Measurement Screen variables are described below. The number of VD steps is defined in the Measurement Section field.

VGS_start	Starting value of the Gate voltage sweep range.
VGS_stop	Stop value of the Gate voltage range.
VDS_start	Stating value of the Drain step voltage.
VDS_step	Step value of the Drain voltage.
V_start	Starting value of the Body second step voltage.
V_step	Step Body voltage value for the second step.
V_points	Number of Body voltage steps.
VBackGate	Constant Backgate voltage value.
points	Number of sweep data points.
wait	Wait time in microseconds, between measurements.
compl_smu(A)	SMU current compliances.
VS	Constant Source voltage.
compl_vs(A)	Current compliance for voltage sources.

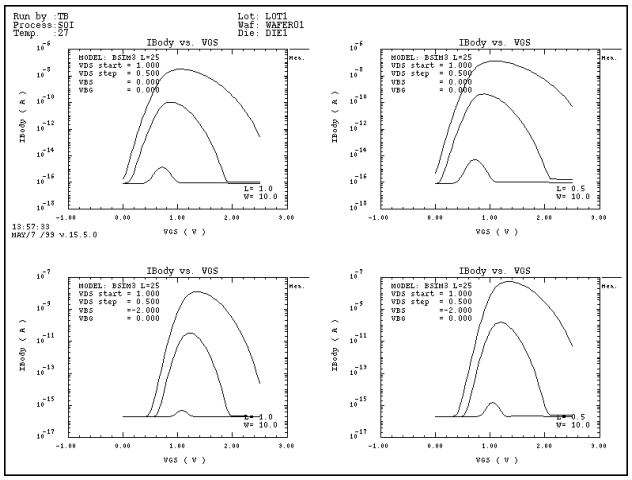

Figure 7. Typical Impact Ionisation current characteristic for several devices and several Body bias.

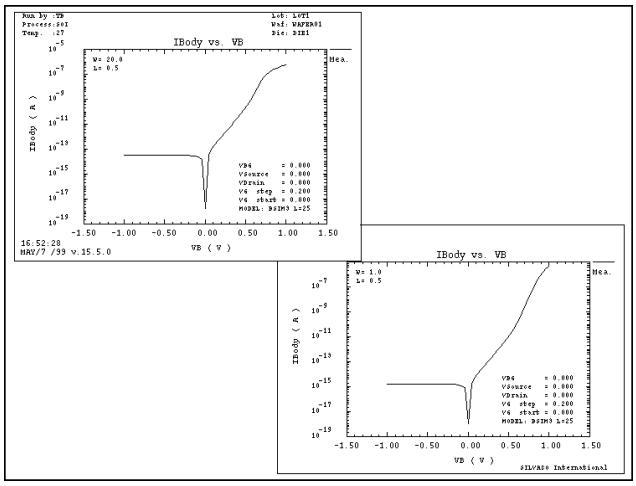

Figure 8. Typical IB(VB) characteristic, for two devices.

IB/VB_MG routine

This new routine is dedicated to measure the well known SOI IB(VB) characteristic. This characteristic represents the current flowing through both Drain-Body and Source-Body diodes. The principle of this measurement is to fix source, drain and BackGate voltages, sweep the Body voltage for several gate bias, and measure the Body current. Also, a classical diode characteristic will be obtained. This routine is a multi-geometry routine, in which measurement, simulation, optimization, rubberband and modeling are available.

The DC Measurement Screen variables are described below. The number of VG steps are defined in the Measurement Section field.

VB_start	Starting value for the Body voltage sweep range.
VB_stop	Stop value for the Body voltage range.
VG_start	Starting value for the Gate step voltage.
VG_step	Step value for the Gate voltage.
points	Number of sweep data points.
VDcst	Constant Drain voltage value.
VScst	Constant Source voltage value.
VBGcst	Constant Backgate voltage value.
compl_smu(A)	SMU current compliances.
compl_vs(A)	Current compliance for the voltage sources.
wait	Wait time in microseconds, between measurements.

IC/VCE Routine

This new routine is dedicated for parasitc Drain-Body-Source Bipolar device characterization. The aim of this routine is to measure the output characteristic of this parasitic bipolar, such as IC(VCE) characteristic for a real Bipolar device. To adapt this for the parasitic bipolar of the SOI device, the drain current for a defined drain sweep voltage should be measured, for several Body bias. We can consider the drain as the collector, the source as the emitter, and the body as the base of an equivalent real bipolar device. This routine is a multi-geometry routine, for which measurement, simulation, optimization, rubberband and modeling features are available.

The DC Measurement Screen variables are described below. The number of VB steps is defined in the Measurement Section field.

VD_start	Starting value for the Drain voltage sweep range.
VD_stop	Stop value for the Drain voltage range.
VB_start	Starting value of the step Body voltage.
VB_step	Step voltage value for the Body steps.
points	Number of sweep data points.
VGcst	Constant Gate voltage value.
VScst	Constant Source voltage value.
VBGcst	Constant BackGate voltage value.
compl_smu(A)	SMU current compliances.
compl_vs(A)	Current compliance for voltage sources.
wait	Wait time in microseconds, between measurements.

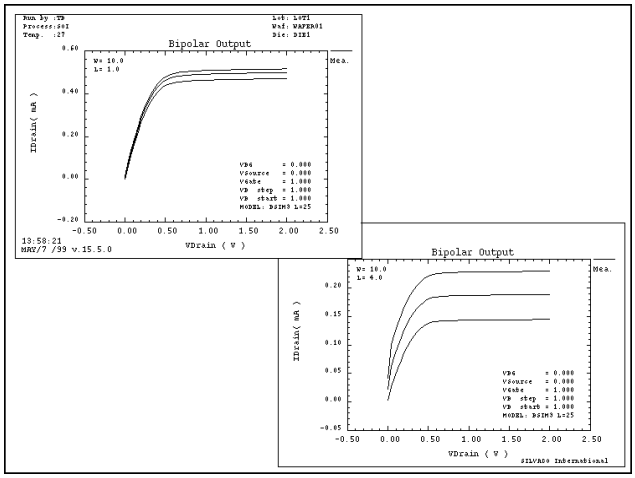

Figure 9. Typical SOI Parasitic Bipolar Output characteristics, for two devices.

DIODE Routine

This routine is again a completely new routine. Its origin comes from the IB/VB_MG routine, in which we measured the current flowing through both Drain-Body and Source-Body diodes. The objective of this Diode routine is to isolate the current of one diode, short-cutting the second one. We can measure the Drain-Body (respectivelly Source-Body) diode current for a defined Body voltage swep range. The principle simple. The same voltage on both Body and Source (respectivelly Drain) terminals; needs to be applied so that the Source-Body (respectivelly Drain-Body) diode will not be biased, preventing current from going through this diode. For measurement, the principle is to use the VAR1', functionnality of the HP4145 and HP4156 instruments. During all measurements, BackGate and Drain (respectivelly Source) are kept to constant values. This measurement can be repeated for several gate voltages, in order to eventually includes the effect of gate biasing on this characterisic. In terms of simulation, the nodes for Body and Source (respectivelly Drain) should be the same. This routine is again a multi-geometry routine, with measurement, simulation, optimization, rubberband and modelling features available.

The DC Measurement Screen variables are described below. The number of VG steps is defined in the Measurement Section field.

VB_start	Starting value for the Body voltage sweep range.
VB_stop	Stop value for the Body voltage range.
VG_start	Starting value of the step Gate voltage.
VG_step	Step value for the Gate voltage.
points	Number of sweep data points.
VDcst	Constant Drain voltage ; only used if VAR1', D=0S=1 is set to 1.
VScst	Constant Source voltage ; only used if VAR1',D=0S=1 is set to 0.
VBGcst	Constant BackGate voltage.
compl_smu(A)	SMU current compliances.
compl_vs(A)	Current compliance for voltage sources.
wait	Wait time in microseconds, between measurements.
VAR1',	D=0S=1 If 0, VAR1', is applied on Drain, and Source-Body diode current is measured. If 1, VAR1', is applied on Source, and Drain-Body diode current is measured.

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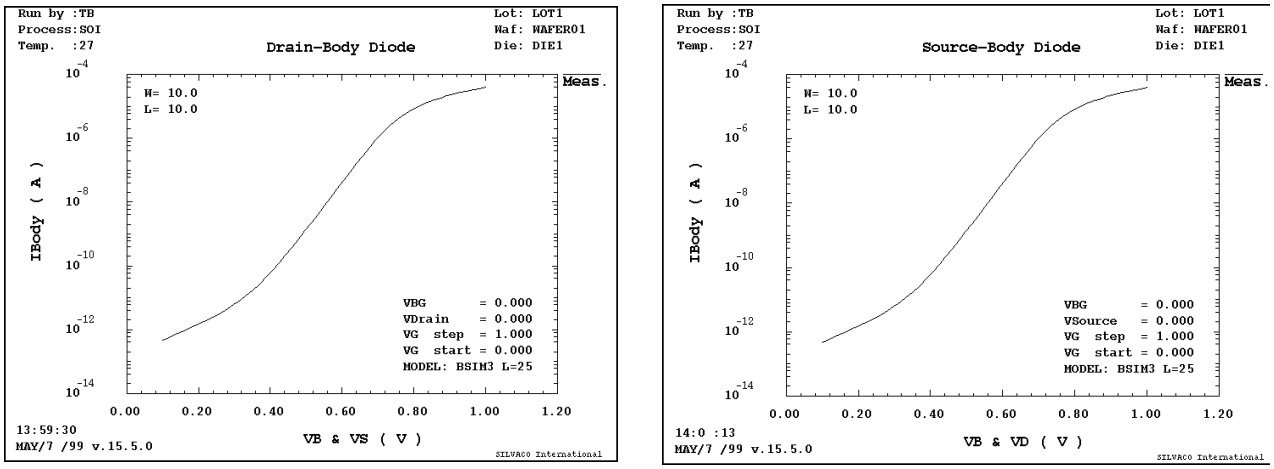

Figure 10. Typical Drain-Body and Source-Body diode current characteristics.

MOS31 JFET/MOSFET Model Now Available in *SmartSpice*

Introduction

Silvaco now offers the MOS31 JFET/MOSFET model originally developed by Philips [1] as part of the ***SmartLib*** product-independent model library. This model is available within ***SmartSpice*** as level 31.

The MOS31 JFET/MOSFET model is an integral part of a high voltage MOS macro-model. This long channel JFET/MOSFET model has been especially developed to describe the lightly doped drift region of LDMOS, EPMOS and VDMOS devices. Both vertical and lateral versions of DMOS exist. The vertical device has the greater current-carrying capability and is mainly used as a discrete device in high-power applications. The lateral type serves as an output driver in high-voltage and power ICs.

Physical Effects

The main effects modeled in this MOS31 model are described below :

- Accumulation at the surface (MOSFET)
- Depletion from the surface
- Depletion from the bulk
- Pinch off mode
- Velocity saturation in the channel
- Gate charge model
- Substrate charge model
- Noise model

Simulation Model

The MOS31 model has only 14 physical parameters (RON, RSAT, VSAT, PSAT, VP, TOX, DCH, DSUB, VSUB, VGAP, CGATE, CSUB, TAUSC, ACH), 2 flicker noise parameters (KF, AF). The SI units are used and the new Philips velocity saturation model has been implemented by default. The gate oxide thickness TOX leads to choose between a MOSFET device (TOX>0) or a device without depletion at the surface (TOX<0).

DC Static Model

The model parameter VERSION has been implemented in order to choose the Philips velocity saturation model. By default, VERSION=30.2. The old Philips models is still available (VERSION=30.0). The dc characteristics are plotted on Figure 1 for both calculation method (ids -vds) and on Figure 2 (ids - vgs). The drain current still increases with drain voltage due to the velocity saturated current flow.

The electrical circuit of DMOS model consists of a low voltage MOS9 in series with one MOS-FET device

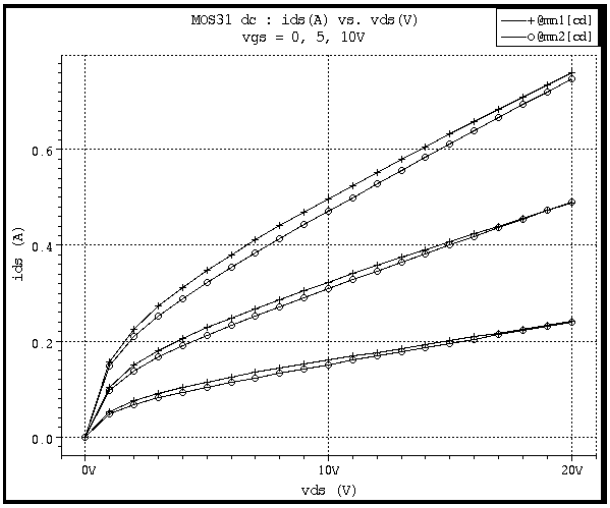

Figure 1. MOS31 dc simulation with version=30.0 (@mn1[cd]) and version=30.2 (@mn2[cd]).

MOS31. An example of its characteristics is plotted on Figure 3 for direct and reverse biases. In agreement with the technology, the results are dissymmetrical.

Noise Model

SmartSpice Common Equations for the 1/f and the shot noise are available using NLEV flag.

Ouput Device Variables

Usual device output variables for MOS31 model like node currents, conductances, various charges and capacitances can be printed, stored and/or measured.

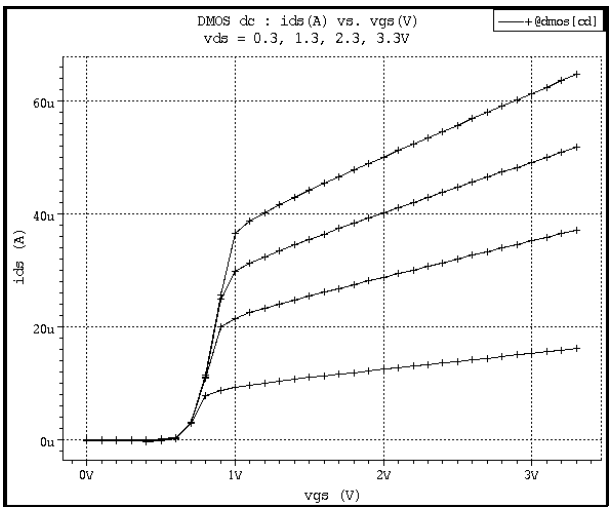

Figure 2. DMOS dc simulation. @dmos[cd] versus vgs.

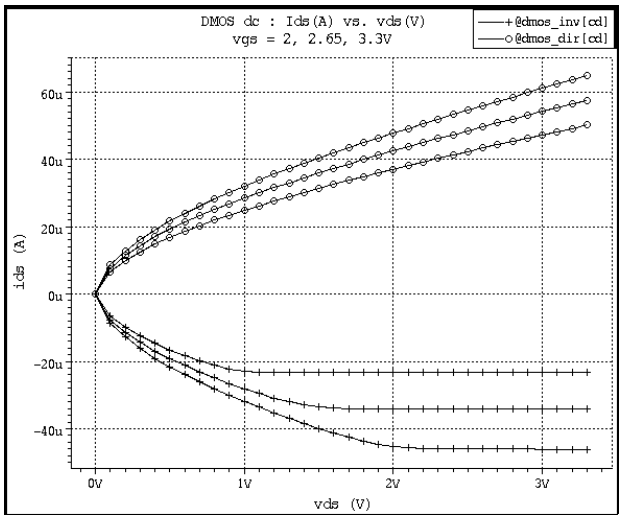

Figure 3, DMOS dc simulatioln. @dmos_inv[cd] versus vds for for reverse bias and @dmos_dir[cd] versus vds for direct bias.

Extrinsic Model

The MOS31 model describes only the intrinsic part of a MOS transistor. The extrinsic part may be evaluated using the ***SmartSpice*** Common Equations. ***SmartSpice*** Area Calculation Method is also supported. By default, the overlap capacitances, bulk source and bulk drain conductances and junction currents are not calculated. Please refer to Silvaco documentation for a complete description [2].

"LEVEL=30 leads to use the model parameters in centimeter whereas LEVEL=31 leads to use the model parameters in meter."

References

[1] A complete description of the model can be found at the following internet address: http://www-us.semiconductors.philips.com/Philips_Models/

[2] *SmartSpice/UTMOST III MOdeling Manual Volume 1* (Silvaco International)

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Gummel Routine

This is a new routine dedicated, as is the IC/VCE routine, to the parasitic bipolar characterization. In order to characterize completely this bipolar, in addition to the output characteristic, the Gummel characteristic should be analyzed. For a classical bipolar device, this characteristic is composed of the Base and Collector curves versus a Base voltage sweep. For this SOI module, the equivalent is to measure the Body (for Base) and Drain (for Collector) currents for a defined Body (for Base) sweep voltage range. During all measurements, Drain, Source, Gate and BackGate are kept to constant values. As all other routines, this is a multi-geometry routine, in which measurement, simulation, optimization, rubberband and modeling features are active. The DC Measurement Screen is described below.

VB_start	Starting value for the Body voltage sweep range.
VB_stop	Stop value for the Body voltage range.
VDcst	Constant Drain voltage value.
VScst	Constant Source voltage value.
VBGcst	Constant BackGate voltage value.
points	Number of sweep data points.
compl_smu(A)	SMU current compliances.
compl_vs(A)	Current compliance for voltage sources.
wait	Wait time in microseconds, between measurements.

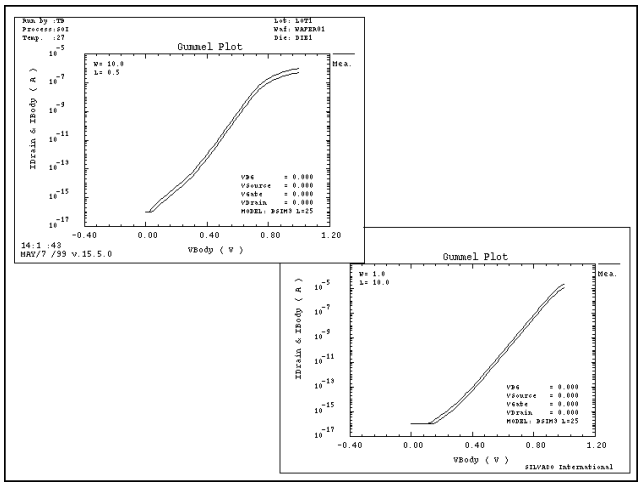

Figure 11. Typical Gummel characteristics for SOI parasitic Bipolar for two devices.

Conclusion

This new SOI module is now available in ***UTMOST III***, and in addition to the various SOI models of ***SmartSpice***, will allow our users to extract a full scalable DC SOI model. The main characteristics are now available in ***UTMOST***, all available in measurement, simulation and optimization, to allow maximum flexibility for users. Rubberband, Modeling and Log Files features are also available.

Calendar of Events

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Bulletin Board

NSREC '99

Silvaco enters the final frontier of success at the National Space and Radiation Effects Conference. Take your designs where no engineer has gone before at this July 12-16 conference in Norfolk, VA.

Spotlight on Systems Education

MSE '99 and Silvaco International join forces for the premier conference for educators in Microelectronic Systems. Our East Coast team will be present to continue our commitment to education.

IC the future of CAD
...and it is Silvaco!

ICCAD `99 hosts Silvaco International's Exhibition suite November 8th-10th. View the NT CAD tools that will revolutionize the next generation CAD market.

Earth shattering circuit simulation, design and verification, parasitic resistance and capacitance in interconnect are just a few of our breakthroughs.

Visit us in Suite **957** Monday, Tuesday, and through lunch on Wednesday for demonstrations.

For more information on any of our workshops, please check our web site at ***http://www.silvaco.com***

Hints, Tips and Solutions

Mustafa Taner, Applications and Support Engineer

New Binning Routine

The "Binning" routine in ***UTMOST III*** MOS module has been greatly enhanced. The bin models can be generated much faster and the routine requires less user interface.

The binning methodology is used when a single scaleable model can not fit all geometries. For such cases a single model is extracted for each geometry and binning methodolgy is applied to generate "L", "W" and "P" term parameters. Four single geometry models are used to generate one bin model. The continuity between the bin models are guaranteed by using the parameters LMIN, LMAX, WMIN, WMAX, LREF and WREF.

The user can enter the number of bins and each bin's geometry information (W, L, Wref and Lref) in the new binning routine's "Model Binning Setup Screen" (Figure 1.).

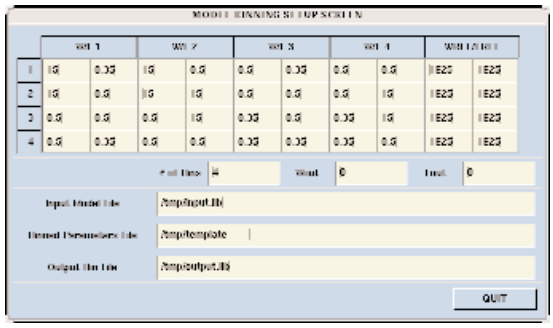

Figure 1. Model Binning Setup Screen.

The input model file should contain all single geometry models. Selecting the correct model from the input model during the binning process is accomplished by comparing the W and L data in the Model Binning Setup Screen and W and L data in the comment line of the input model file. The comment line with W and L data should be present before the ".model" statement of each model. ***UTMOST III*** library generation feature has been modified to add a comment line including the W and L values when there is only a single device selected in the model strategy screen (Figure 2.)

```
.LIB TT
* DATE: Oct  4/99
* LOT: SILVACO                WAF: 1
* DIE: 1                      DEV: 1
* Temp= 27
* W=   15.0 L=   15.0
.MODEL N15x15 NMOS (                                LEVEL   = 8
+VERSION = 3.1            TNOM     = 27             TOX     = 7.5E-9
+XJ      = 2E-7           NCH      = 2.560743E17    VTH0    = 0.6182272
```

Figure 2. Single Geometry model including W and L information.

Call for Questions

If you have hints, tips, solutions or questions to contribute, please contact our Applications and Support Department

Phone: (408) 567-1000 Fax: (408) 496-6080

e-mail: *support@silvaco.com*

Hints, Tips and Solutions Archive

Check our our Web Page to see more details of this example plus an archive of previous Hints, Tips, and Solutions

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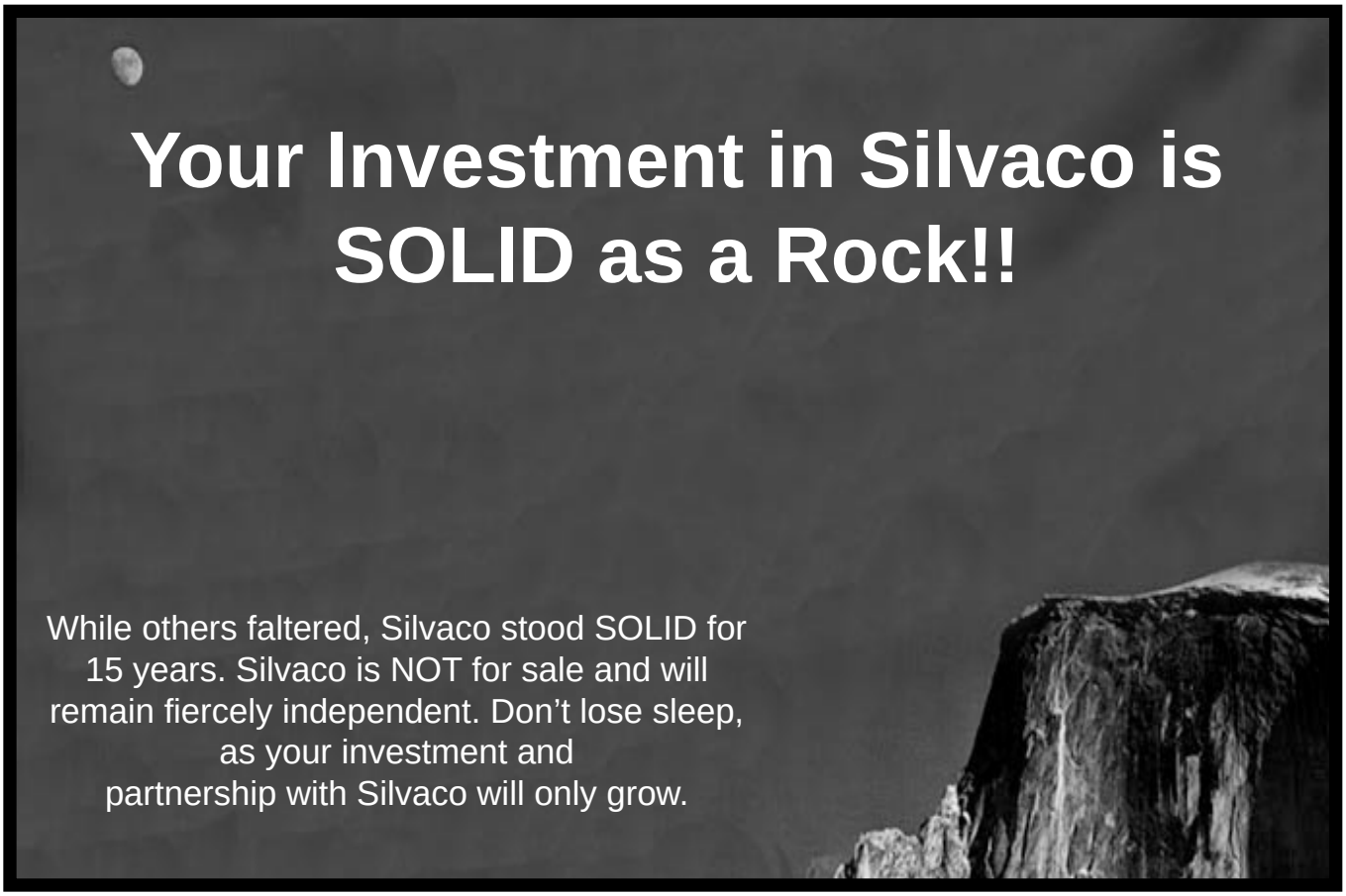
The "Binned Parameters File" contains the name of the parameters with "+" or "-" signs as prefixes. (Figure 3.) The "+" sign indicates that the following parameter will be used for binning. The parameters with "-" prefix are kept constant and "W", "L" and "P" terms are not generated (Parameters such as TOX, XJ, NCH, etc usually have "-" prefixes).

```
-LEVEL
-VERSION
-TNOM
-TOX
-XJ
-NCH
+VTH0
+K1
+K2
-K3
```

Figure 3. Part of a "Binned Parameters File" used for binning

The "Output Bin File" contains all bin models. After the generation of the Output Bin file, parameters LMIN, LMAX, WMIN, WMAX, LREF and WREF are added to each bin model automatically.

A reverse operation of generating a single geometry model from a bin model can be performed too. An input model file which contains bin models should be entered in the "Input Model File" field of the "Model Binning Setup Screen". The values for "Wout" and "Lout" should be entered for the target single geometry model. The "Output Bin File" field is used as the Output Single Model file name for generating a single geometry model.



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