Simulation Standard

TCAD Driven CAD

A Journal for Process and Device Engineers

Generating a Capacitance Coefficient Database for any Chip Level LPE Tool Using *EXACT*

1.0 Introduction

EXACT is a sophisticated interconnect characterization tool integrated into the ***DISCOVERY*** framework. It is designed to build the capacitance coefficient database required by any Layout Parasitic Extraction (LPE) tool. To calculate these coefficients accurately, an internal 3D process simulator creates test structures, such as shown in Figure 1. Then an integrated 3D field solver calculates the capacitance for each device layer and test structure combination. A simple internal script language then reformats the capacitance database so that it can be used with *any* chip level LPE tool.

This article is split into two sections. The first section describes the general program operation used for ***EXACT*** and the second section in a later issue of the *Simulation Standard* will describe examples of it's use.

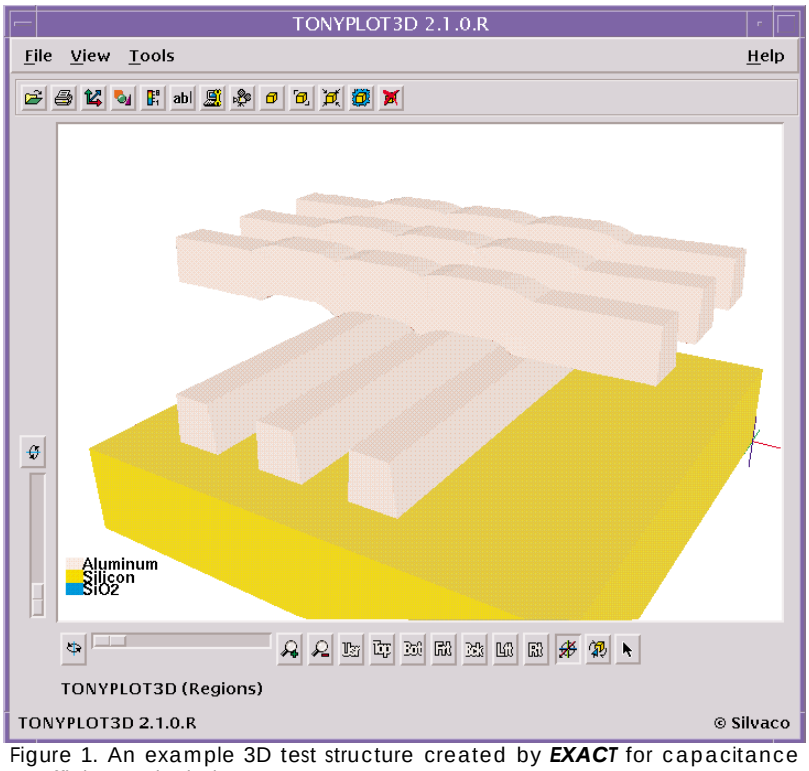

Figure 1. An example 3D test structure created by ***EXACT*** for capacitance coefficient calculations.

1.1 Why Is There A Need To Accurately Model Interconnects?

For large geometry device designs, the circuit timing delays are primarily due to the active devices. In other words, for large geometry designs, if the switching speed of the active devices is improved, the circuit delays are also improved. This situation, however, is not the case for sub-micron designs. As the technology geometry size shrinks parasitic delays from the interconnect dominate the delays originating from the active devices.

It is no coincidence that a large research effort has been directed towards researching new ways of reducing inter-connect capacitance, such as using copper and LoK materials. In today's technology, interconnect capacitance parasitics are limiting improvements gained by advances in active device design and packing density.

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INSIDE

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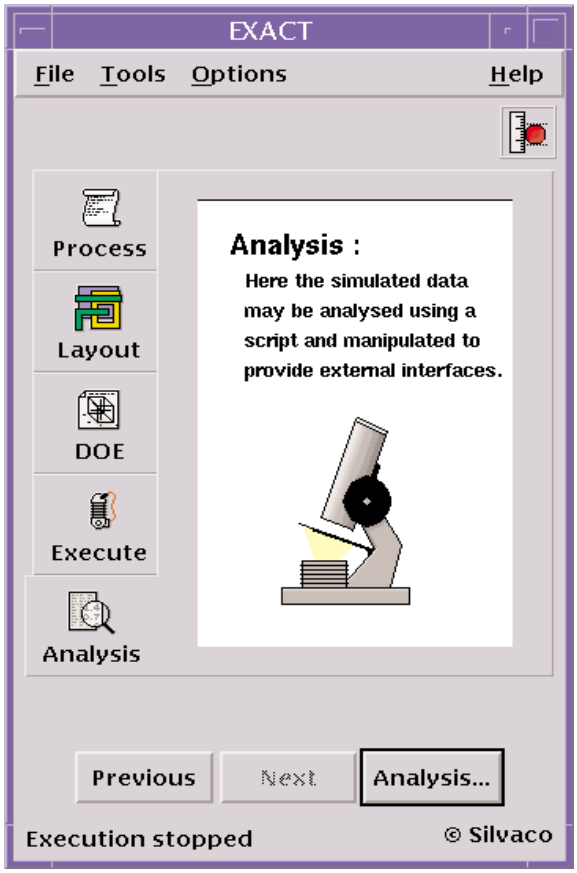

Figure 2. Exact Main GUI Showing the Five Experimental Steps

What is required is a new tool to accurately model interconnect geometry using 3D processing and a physics based 3D field solver that can be used in the inter-connect optimization process, to simulate trial and error iterations in connectivity designs, *both* for Layout and Process improvements. A tool that is easy to use and can be interfaced to existing LPE software to greatly speed up the learning curve and reduce experiments to a few days. ***EXACT*** provides these capabilities.

1.2 What Is Wrong With Capacitance Information Provided By The Foundry?

Seasoned users of full chip Layer Parasitic Extract (LPE) tools will be aware that the parasitic capacitance information provided by most foundries, although accurate, is usually very limited in nature. Often the inter- and intra-layer interconnect capacitance is provided for each layer for lines of minimum width and minimum spacing only. It would be an unusual design that only consisted of conducting lines of minimum width and minimum spacing. If any lines were not of minimum width and minimum spacing on the chip, the full chip LPE tool has to guess what the capacitance should be or ignore it altogether. This can lead to significant inaccuracies in the extracted parasitics which inevitably leads to inaccuracies in chip timing predictions.

Using ***EXACT***, the design engineer can now calculate the capacitance between lines for any width and any spacing and for any process variation between any combination of layers. The capacitance database available to the full chip LPE tool can be as complete as the user wishes it to be. Greater accuracy and predictability is the result. It is now possible to investigate the effect of different design and process philosophies in software, thus greatly improving the time taken to optimize circuit design and time to market of the product.

The limited measured data from the fabrication house can be utilized to double check the accuracy of the predictions from ***EXACT***.

2.0 EXACT Capabilities

EXACT is a flexible tool that can perform a large matrix of experiments accessible from a user friendly Graphical User Interface (GUI). The Design Of Experiments (DOE) can consist of any mix of process and layout variables. Variables such as etched sidewall angle, stepper optical source wavelength, film deposition isotrophy, insulator permittivity, multiple non planer insulator structures

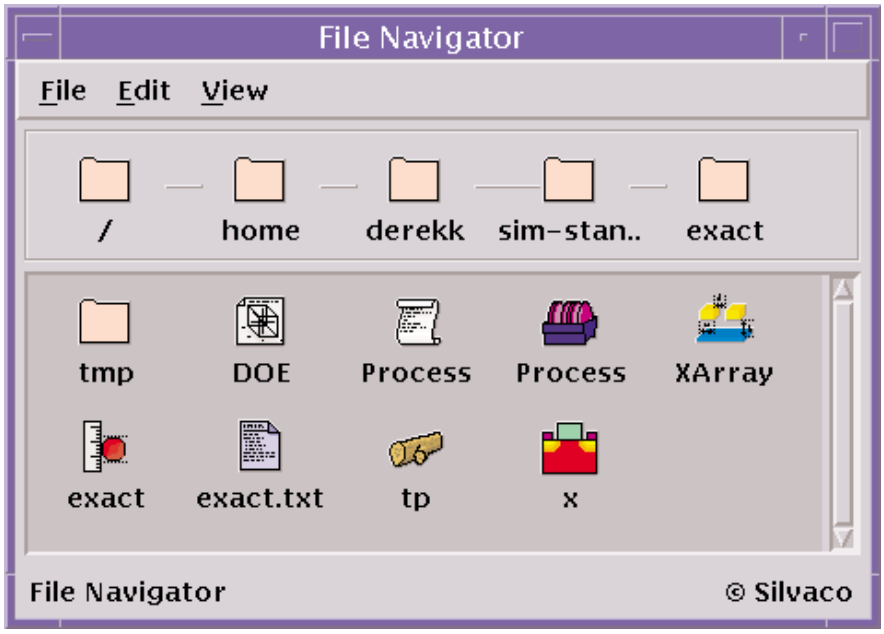

Figure 3. Exact "Matching Icon" Drag and Drop File Manager

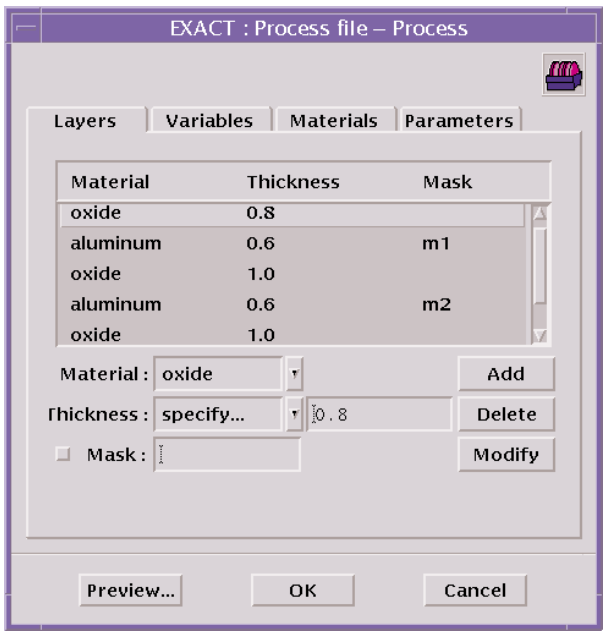

Figure 4. The Standard Mode Interactive GUI for Input of Layer Properties

layers, insulator thicknesses and general line width and spacings can all be incorporated into a single or multiple large Design Of Experiments (DOE) which typically consists of several thousand individual experiments.

The processing options in ***EXACT*** are geometric etches and depositions, or realistic etching and deposition. An integral optical solver allows photolithography effects to be taken into account, together with the exposure level at which the photoresist will develop. All relevant properties of the realistic etching, deposition and optolithographic models are user definable, including the degree of isotropy of an etch or deposition, the wavelength, aperture and shape of the exposure source, the critical intensity at which the photoresist will develop.

Users of a pre-optimized foundry process will usually have a design of experiments (DOE) that would consist of layout variables such as width and spacing. Once a technology has been fully characterized, the created data base can be used with *any* full chip LPE tool by manipulating the data base with a simple but powerful script language. The script language enables the user to write a complete LPE rule file. The script language can output text, manipulate rows and columns of the database, delete, add or modify rows and columns and fit the data to user specified formula, output the data as an LPE rule file or in graphical, Excel or text table format. This ensures that ***EXACT*** is future proof for any new chip level LPE tool that comes on the market.

3.0 Using EXACT

When starting ***EXACT*** presents the user with a intuitive Graphical User Interface (GUI) as shown in Figure 2. The main GUI provides the user with five main folders corresponding to the five distinct stages of generating a database.

The five stages are:

Stage 1: Process Information - Layer thicknesses and film properties

Stage 2: Choosing test structures - Layouts & layer combinations required

Stage 3: Design of Experiments - setting chosen variable values

Stage 4: Execute the calculations

Stage 5: Analyze, manipulate and visualize the generated database

Each stage of the procedure has a corresponding icon which opens the relevant GUI for that particular section of the experiment. The whole ***EXACT*** experiment or

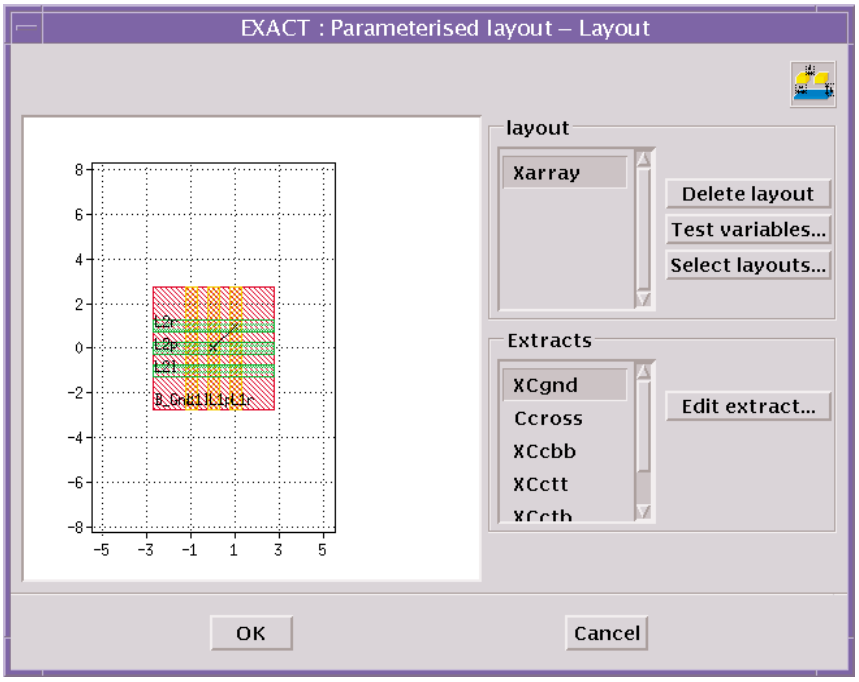

Figure 5. The Layout GUI, Showing a Typical, Pre-defined Standard Test Layout

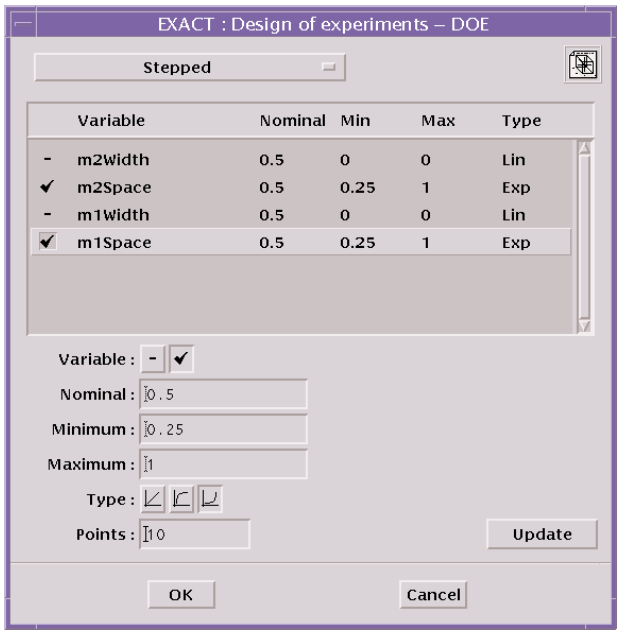

Figure 6. The design of experiments GUI, showing selection options for metal width and space.

any individual stage of the experiment, can be saved or loaded from the "drag and drop" style file manager which displays the files as icons that match the icon representing any individual stage as shown in Figure 3.

EXACT has two modes of operation, standard and advanced. In standard mode, Interactive menus create the required files or pre-defined files are simply loaded via the "drag and drop" file manager facility. In advanced mode, the user has access to the files created and can modify them using the ***EXACT*** or any other text editor. Advanced mode also offers structure layout modification or creation facilities not available in standard mode. The user can switch between standard and advanced mode at any stage of the experiment.

Process Definition

The following GUI examples are using standard mode operation. The process GUI allows simple interactive input of layer thickness, material properties and parameters that are required to be variable. Each subject is brought to the foreground by clicking on the relevant folder heading as shown in Figure 4.

Test Structure Definition

Once the device layers have been defined, the mask layout designs of the required test structures are chosen using the Layout GUI as shown in Figure 5.

The number of test structure types required depends on the complexity of the device models. For example, a reasonably accurate device model can be obtained with just two test structure types which allow extraction of overlap capacitance, layer to layer fringing capacitance and same layer fringe capacitance for any layer combinations and any space and width combinations.

The versatility of the program results from the parameterization of each test structure layout. The test structure dimensions are not defined as constants but as variables. Thus, in the interactive GUI, you can use the same base test structure layout but vary the spacing and widths in the structure. The test structure can also be defined in any combination of the layers using the interactive GUI interface. It is possible to design a comprehensive design of experiments encompassing every possible variation of line width, spacing and layer combination with a few entries in the interactive GUI.

Design of Experiment

Users do not have to enter every spacing or width you require. Simply enter the initial value, final value, number of points and how you wish to space these experimental points (either linearly, logarithmically or exponentially) as shown in figure 6.

The user can control running the experiments from the Execution control window, shown in Figure 7.

Analysis and LPE interface

On completion of all the experiments, the analysis window is displayed as shown in Figure 8. In standard mode, the user can “drag and drop” a standard script

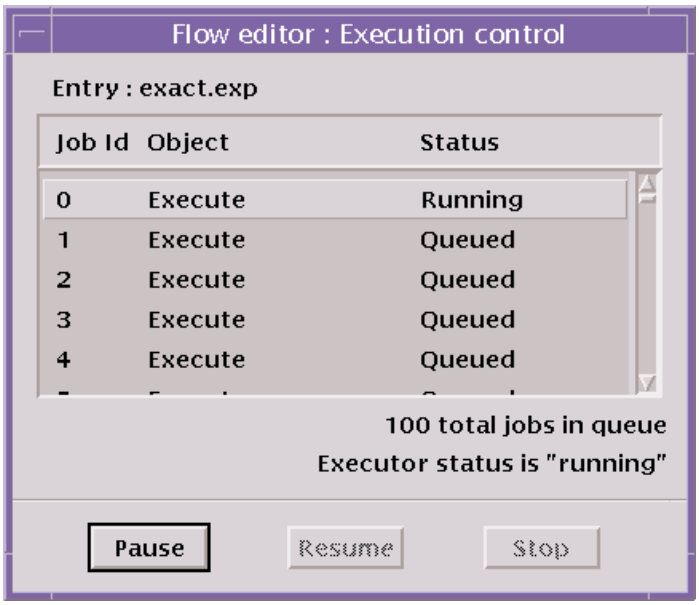

Figure 7. The Exact Runtime Window is updated in real time.

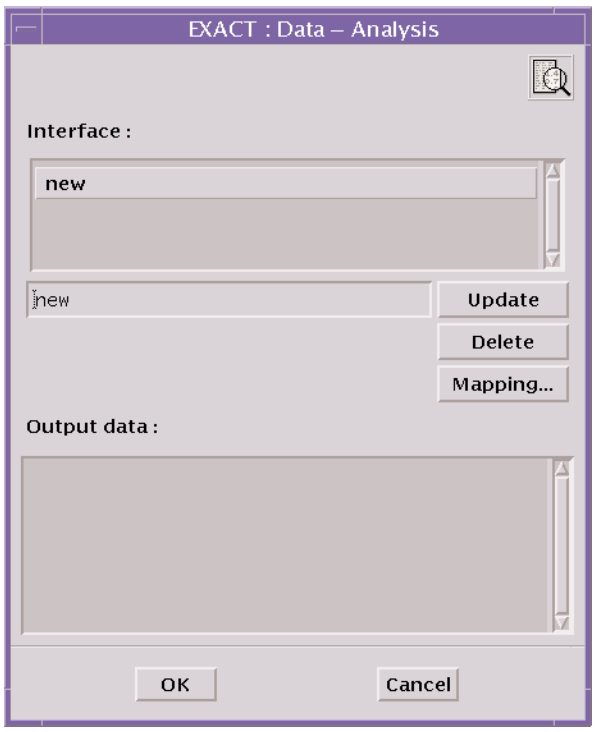

Figure 8. The Analysis Window allows multiple types of export of capacitance data.

nential spacing option discussed above. The exponential option uses smaller steps near the minimum geometry for greater accuracy where the parasitic capacitance is greatest.

More details on ***EXACT*** database manipulation using the provided script language is the subject of the next Simulation Standard article in the following issue.

4.0 Conclusion.

EXACT provides a simple way to create a comprehensive and accurate interconnect parasitic capacitance database. ***EXACT*** creates the database using a 3D process simulator and 3D field solver in a self-contained package. The creation of a comprehensive database increases the accuracy of the full chip LPE tool that is used to extract circuit parasitics. ***EXACT*** can be used with *any* LPE tool using the script language or the ready made conversion scripts provided. There are no limits on the process complexity of test structures allowed in. ***EXACT*** can account for complex non planar processing and unusual or special structures in the chip layout.

to create the active section of a full chip LPE rule file. In advanced mode an ***EXACT*** text editor is displayed which allows modification or creation of a script to act on the calculated data base. In its simplest form, an advanced script could consist of a single line to dump the database into a text table. The script file to do this would be:

```
dump @file=<filename>
@format=table
```

If the user wished to look at and manipulate the data in Microsoft's Excel, the script file would be simply:

```
dump @file=<filename>
@format=csv
```

Figure 9 shows an output using the graphical format plotted using ***TonyPlot***. The plot is a result of changing the spacing of the bottom metal stripes of the test structure shown in Figure 1 from 0.25µm to 1.0µm in 20 steps using the expo-

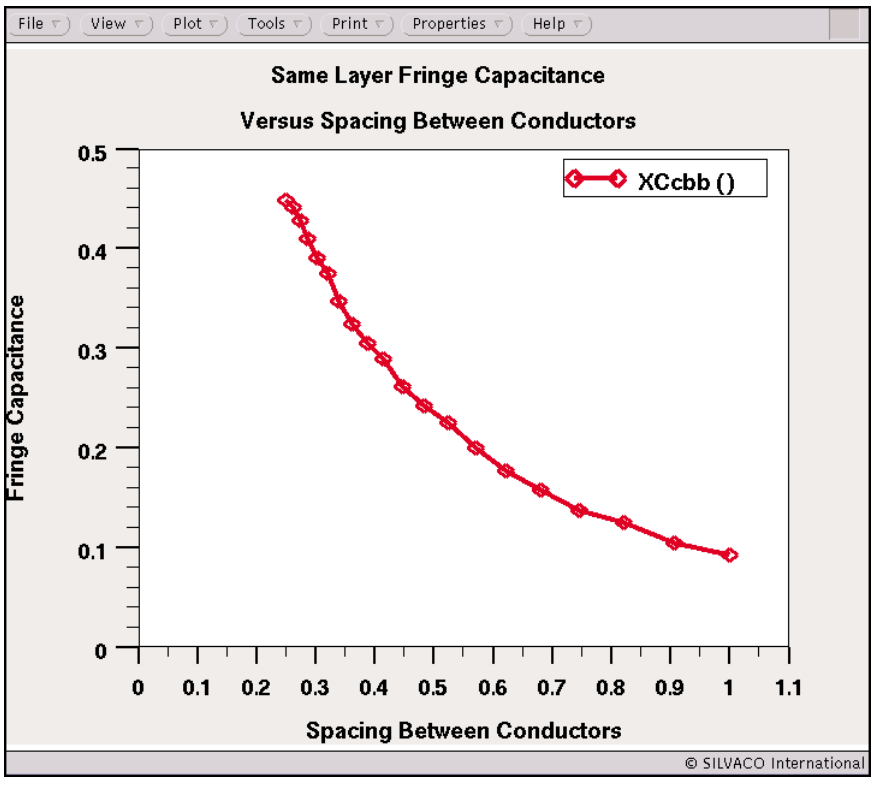

Figure 9. Same Layer Fringing Capacitance versus Line Spacing .

New Thermionic Emission and Tunneling Models in *ATLAS*

Introduction

In order to simulate heterojunction devices accurately, both the thermionic emission and tunneling mechanisms must be considered when calculating transport across hetrojunctions. Drift-diffusion descriptions of carrier mobility are incomplete at abrupt heterointerfaces. New thermionic emission and tunneling models have been incorporated into ***ATLAS***. This paper discusses the models and presents two examples of device simulation.

Descriptions of the thermionic emission and tunneling across a heterointerface were presented by Yang et al.[1] They developed a thermionic-field emission boundary condition based on the WKB approximation. These models for thermionic emission and thermionic-field emission (tunneling) across a heterointerface have been incorporated into ***ATLAS***.

Current-voltage characteristics for two devices are analyzed as a function of doping, composition and temperature and are compared to data in [1].

nN Heterojunction Device

Carrier transport in an isotype nN heterojuction device is presented. Current due to thermionic emission is significant for nN isotype heterojunctions. These devices show rectifying current vs. voltage characteristics. In reverse bias mode, these devices show varying levels of thermionic emission and tunneling current.

A one-dimensional device was simulated by ***ATLAS***. One region consisted of GaAs with uniform 1e15 /cm^3 n-type dopant, and the second region consisted of $Al_{0.25}Ga_{0.75}As$, with uniform n-type dopant. Three cases were studied, varying the level of uniform doping in the second region. The three values of n-type doping in the second region were 1e15, 1e16 and 5e16 /cm^3. The calculated conduction band profiles under a bias of -0.1 V applied to the first region are shown in Figure 1.

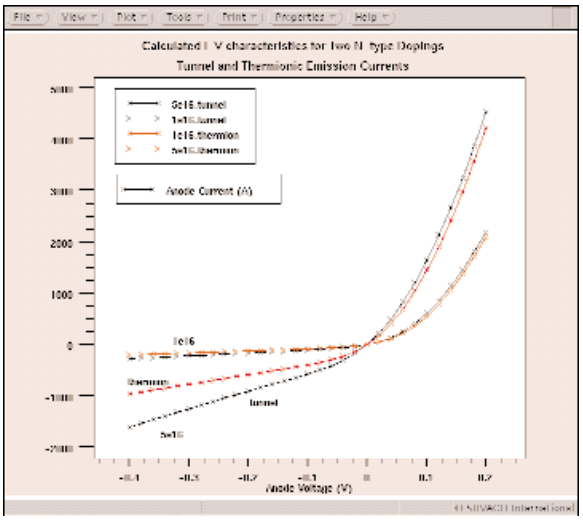

Figure 2: Calculated I-V characteristics of an n-GaAs / n-AlGaAs diode. Units of current are Amps/cm^2.

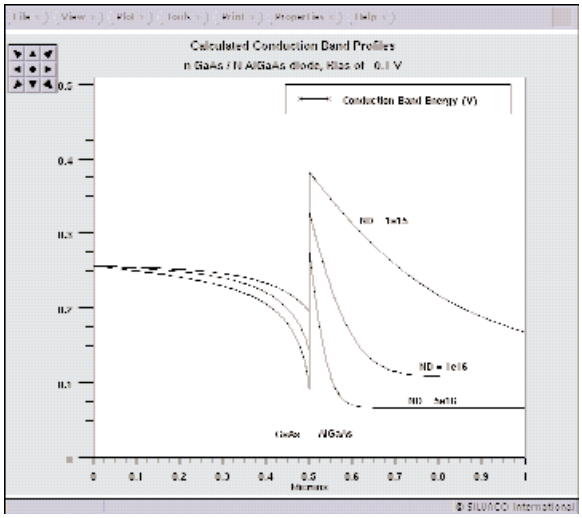

Figure 1: Calculated Conduction Band Profiles for a heterojunction at -0.1V.

In the forward bias condition, the conduction band edge of the second region (AlGaAs) is shifted upward, more electrons go over the barrier, hence increasing the thermionic emission. In the reverse bias condition, the electrons injected from the first region (GaAs) see an abrupt energy barrier whose height is determined by the conduction band discontinuity. At higher doping densities, the peak of the conduction band approaches the Fermi level and the energy barrier becomes thinner. The increase of reverse current with increasing n-type doping in the AlGaAs predicted by the thermionic emission model can described by the lowering of the effective barrier height, hence more electrons going over the barrier. However, as the barrier thickness is reduced, the electrons with lower energy than the barrier contributes to the tunneling current. The I-V characteristics are shown in Figure 2. Units of current are Amps/cm^2.

Additional simulation of a pN device was performed. The current density in both forward and reverse bias conditions as a function of n-type doping was simulated. The dominant mechanism for transport was also thermionic emission. (The results are not shown.)

$Al_xGa_{1-x}As$ Graded Heterojunction Barrier

The current transport of a graded isotype heterojunction barrier was studied and simulation results were compared to experimental measurements. The device consisted of

GaAs - $Al_xGa_{1-x}As$ - GaAs regions, all n-type. The GaAs regions were each 0.25 um thick, and the AlGaAs region was 0.078 um thick. The fractional aluminum composition was linearly graded from 0.3 to zero.

The conduction band profiles of the AlGaAs graded heterojunction barrier diode using the thermionic-field emission (tunneling) model at two biases are shown in Figure 3. In the forward bias case, the electrons are injected from region 3 to region 1 and the barrier height is reduced as the conduction band edge of region 3 moves upward. However, in the reverse bias case, the electrons from region 1 encounter an abrupt energy barrier. The electron transport across the barrier occurs either by thermionic emission over the barrier or by tunneling through it. Since the electron energy barrier becomes more transparent under reverse bias, the tunneling process is expected to dominate as the reverse bias increases.

Simulation and experimental measurements confirm that tunneling becomes the predominant mechanism for electron transport across the barrier in reverse bias. Figure 4 shows the forward and reverse bias current in this device at 300K. The calculated results of both the thermionic emission and tunneling currents are shown. These results follow the trend of experimental results. The predicted I-V rectifying properties of this device are observable.

The calculated results of both the thermionic emission and tunneling currents are shown at two temperatures in Figure 5. There is good agreement between the trend of the tunneling simulation and experimental results. Similar to the nN case, the thermionic emission model significantly underestimates the reverse bias current density and tunneling becomes a dominant conduction process.

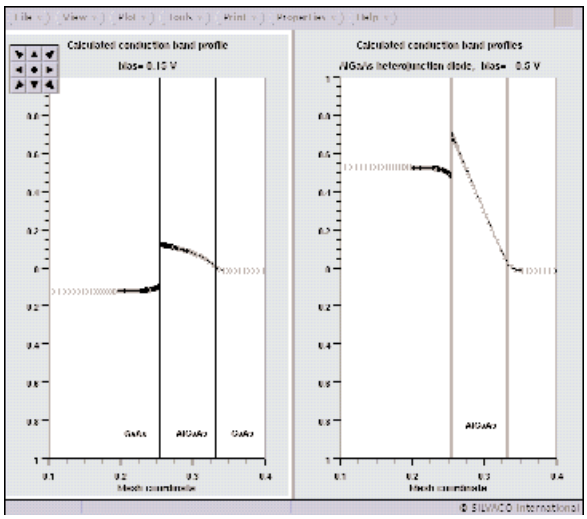

Figure 3: Calculated conduction band profiles of a GaAs - AlGaAs - GaAs diode at bias of a) 0.15 V and b) -0.5V.

Conclusion

New thermionic emission and tunneling models have been incorporated into ***ATLAS***. These models are necessary to simulate heterojunction transport accurately. Simulations of nN GaAs-AlGaAs and isotype graded GaAs-AlGaAs-GaAs heterojunction barriers were presented and compared to published data.

Reference

[1] "Numerical Modeling of Abrupt Heterojunctions Using a Thermionic-Field Emission Boundary Condition", K. Yang, J.R. East and G.I. Haddad, Solid State Electronics, vol. 36, no. 3, pp321-330, 1993].

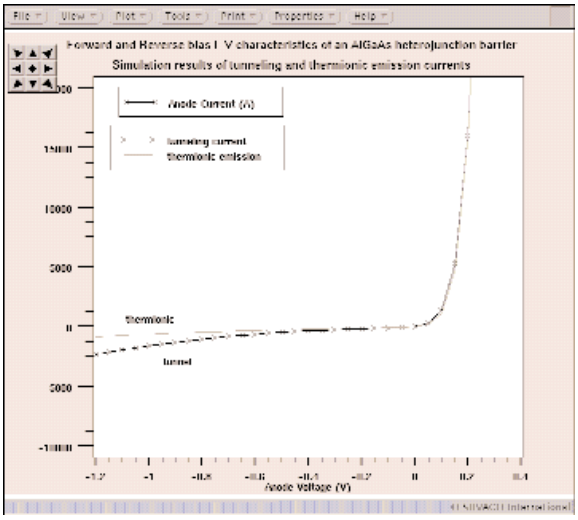

Figure 4: The I-V characteristics of an AlGaAs triangular heterojunction barrier diode at 300K. The calculated thermionic emission current (line) and tunneling current (line and crosses) are both shown.

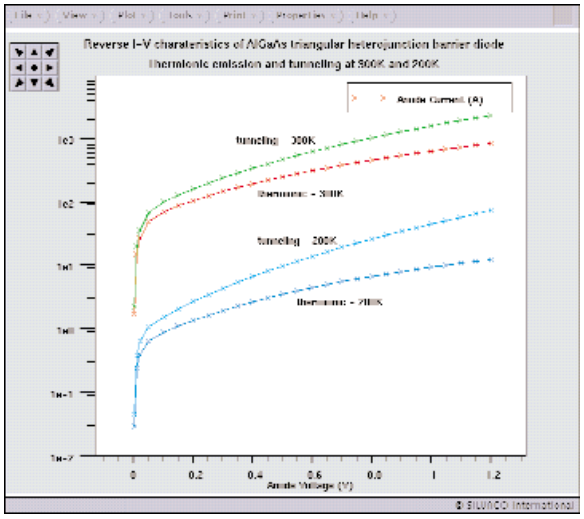

Figure 5: Reverse Bias I-V characteristics at 300K and 200K of thermionic emission and tunneling currents for a graded isotype GaAs-AlGaAs barrier.

High Performance ATHENA and ATLAS Simulation on PC under NT

The recent advances in PC hardware capability in terms of memory and CPU floating point performance has allowed the possibility of running realistic sized ***ATHENA*** and ***ATLAS*** problems on PCs. The Fall 1999 release of PC-TCAD will include all the important features of the latest UNIX release. A product chart showing the modules available on PC is in Figure 1.

The Fall 99 PC-TCAD release is ported to Windows NT4.0. It features PC specific interactive tools based on the popular UNIX products but with the look and feel of true NT products. There is also a dedicated PC Interactive tools manual. A view of the products in action is shown in Figure 2.

One of the most common concerns about ***ATHENA*** and ***ATLAS*** running on PC is the performance.

Six examples from our standard UNIX example set were chosen. These represented a cross section of typical applications:

- MOS shallow junction formation using fully coupled diffusion with {311} implant damage
- SOI Id/Vds using impact ionization, energy balance and lattice heating
- AlGaAs HEMT IV characterization
- BJT switching simulation using ***MixedMode***
- LDMOS power device breakdown including full process simulation
- Power Diode simulation using a large simulation mesh

Each of these files were executed on several different PC hardware configurations. The results are shown in Table 1. Naturally the results show that, as with UNIX, the speed of simulation is strongly determined by the hardware configuration.

Between the Desktop machine and the Notebook the typical speed up was 1.2x which corresponds to the ratio of the processor clock speed. Between the Dual Processor machine and the Desktop the typical speed up was 1.1x which also corresponds to the ratio of the processor clock speed.

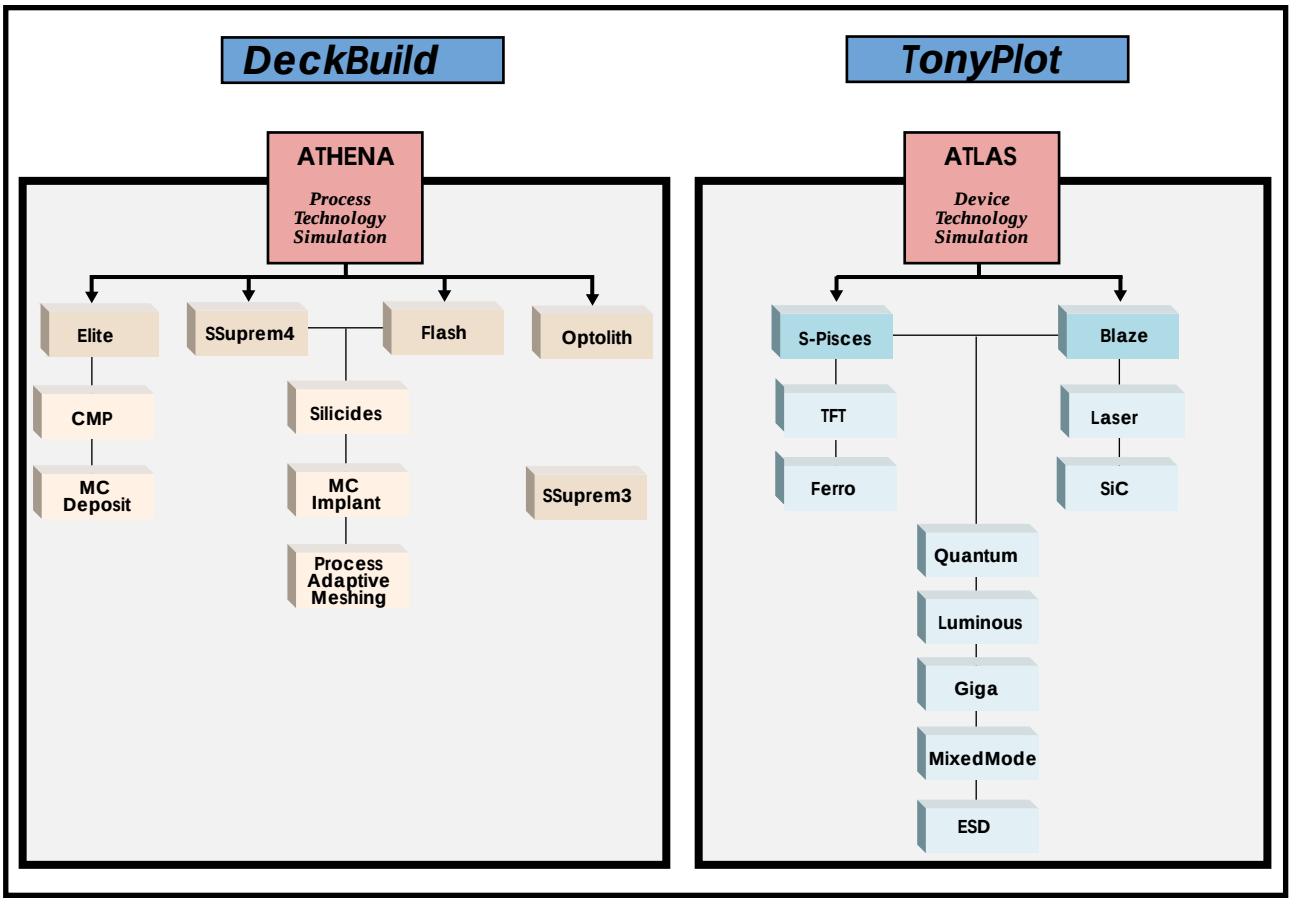

Figure 1. Products available in the Fall 99 release of PC-TCAD.

	PC	Pentium II Notebook	Pentium II Desktop	Dual Pentium III
	CPU SPEED (MHz)	333	400	2 x 450
	MEMORY (Mb)	64	256	1000
EXAMPLE	**Mesh Size**	**Timing (s)**	**Timing (s)**	**Timing (s)**
SOI with Energy Balance and Lattice Heat	1271	1154	919	783
AlGaAs HEMT I_D/V_{DS}	1204	424	329	290
Bipolar Switching in MixedMode	1922	1619	1276	1119
Fully Coupled Diffusion for MOS Junctions	1106	1403	1141	1071
LDMOS Breakdown	2874	3486	2787	2464
Large Power Diode	7659	6611	1248	1167

Table 1. Speed comparison for typical TCAD application examples on various types of PC. All CPU times are in seconds.

The Fall99 release of PC-TCAD tools does not include any specific speedup for dual processor machines. However since the typical task of running simulations involves running a simulator and simultaneously analyzing results in Tonyplot, it would be expected that dual processor machines would offer improved performance for 'interactive' use of the tools as opposed to these purely batch mode timing tests.

However of particular note are the timings for the Power Diode example. This example uses a very large mesh which required 168Mb of virtual memory to run in the UNIX version. The 5x speed up for this example between the desktop and the notebook machines is mostly due to the increased memory in the desktop machine. However between the dual processor machine and the desktop the speedup was similar to the other examples at 1.1x since the 256Mb in the desktop was sufficient. This quantifies the importance of memory to the PC performance on large examples.

Summary

In summary the Fall 99 release of PC-TCAD has been proven to run large, practical process and device simulations in a reasonable time. The CPU time scales linearly with processor clock speed if there is sufficient memory available. With only 64Mb of memory the largest examples will struggle, so a recommended memory of 256Mb will offer the best performance.

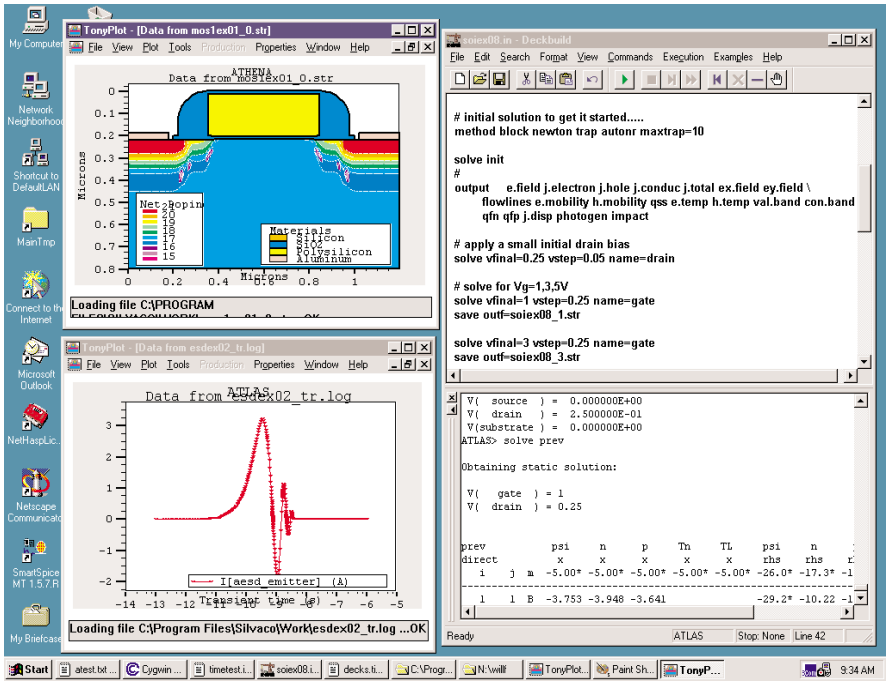

Figure 2. Screenshot of the PC-TCAD Interactive tools DeckBuild and TonyPlot.

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Bulletin Board

3D Ion Implantation

Silvaco software developer, Dr. Ivan Chakarov, presented two papers at the Atomic Collisions Conference in Denmark. Dr. Chakarov impressed the audience with a new technique for trajectory separation of Monte Carlo implant simulation. This technique allows efficient, accurate analytical modeling of 3D implant channeling.

Photomask `99

The power of Silvaco's ***Optolith*** tool is on display at the Photomask conference in Monterey. We will be exhibiting September 15th through 17th at the Monterey Marriott. ***Optolith*** is the industry leader in photolithography design.

Go Crazy For Bipolar!

Our annual trip to BCTM gains more converts every year to the power of Silvaco! Again held in Minneapolis the last week in September, this conference attracts the big league players that determines the direction of the Bipolar industry.

Once again, Silvaco is the 800-pound gorilla in Bipolar design tools!

If you would like more information or to register for one of our our workshops, please check our web site at ***http://www.silvaco.com***

Hints, Tips and Solutions

William French, Applications and Support Manager

Q: How is temperature dependent breakdown voltage modeled in *ATLAS*?

A: Modeling of the increase in breakdown voltage at elevated temperatures requires a model to describe the temperature dependence of the impact ionization coefficients. In ***ATLAS*** there are two impact ionization models that include lattice temperature dependence. They are the Crowell-Sze model[1] called using the command `IMPACT CROWELL` and the Selberrherr Model[2] called using the command `IMPACT SELB`.

Users do not need to explicitly turn on any temperature dependent model. The impact ionization coefficients are always calculated based on the local lattice temperature. The temperature dependence is identical whether the lattice temperature is a uniform elevated temperature set using `MODELS TEMP=<value>` or if the simulation includes lattice heating in ***Giga***.

An excellent recent paper by Valdinoci et al [3] reports on a measurement technique to calibrate such models by measuring diode breakdown at constant elevated temperatures up to 400 °C. This paper proposes a new model which might be prototyped in ***ATLAS*** via the C-Interpreter. However it is informative to compare the reported measured data with the default models in ***ATLAS*** and then to apply tuning to attempt to match the measurements.

Measurements are reported in [3] for p+/n-well diode breakdown at temperatures from 293K to 473K. The doping profile of the diode was estimated from the room temperature breakdown voltage. Simulations were then run with the default coefficients for `IMPACT SELB` and `IMPACT CROWELL`. Results are shown in Figure 1.

The results show the Crowell model does not match the temperature dependence of breakdown voltage. In fact the results match closely those reported in [3] for the same model. The default `IMPACT SELB` results show a better match but under-estimate the effect of temperature on impact ionization by a significant amount. Clearly from the trends of the results, this discrepancy can be expected to grow at even higher temperatures.

By applying the following tuning parameters to the `SELB` model, it was possible to closely match the experimental breakdown versus temperature data.

```
IMPACT MATERIAL=Silicon SELB  A.NT=0.3 \
B.NT=0.248 M.ANT=1.0 M.BNT=1.0
```

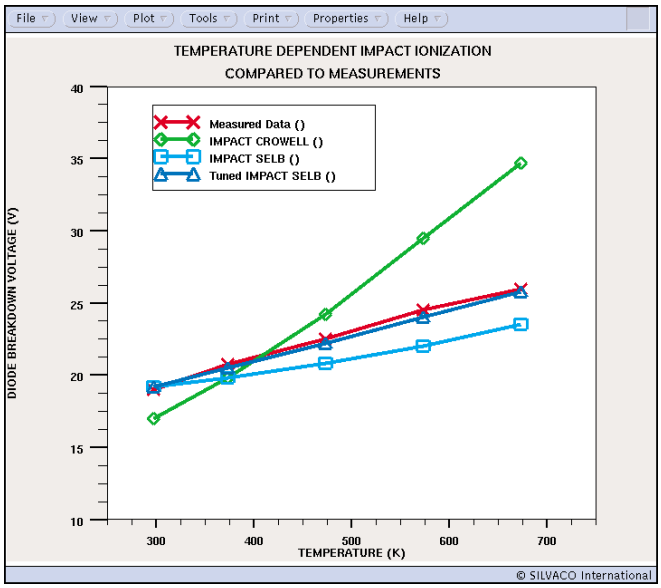

Figure 1. Comparison of default and tuned models in ***ATLAS*** to measured data for breakdown voltage vs. temperature.

Although this calibration is purely empirical, it is useful to fit measured data with the minimum of changes to the existing models. Typically users require only very minor calibration to fit room temperature breakdown voltages. Moving to a completely new model for temperature dependent ionization rates might require recalibration of the room temperature results so re-tuning of existing models a first option.

References

[1] C.R. Crowell, S.M. Sze, "Temperature Dependence of Avakanche Multiplication in Semiconductors", Applied Physics Letters 9, pp. 242-244, 1966.

[2] S. Selberherr, "Analysis and Simulation of Semiconductor Devices", Springer-Verlag, Wien-New York. 1984.

[3] Valdinoci et al. "Impact Ionization in Silicon at larg operating temperature", SISPAD 1999.

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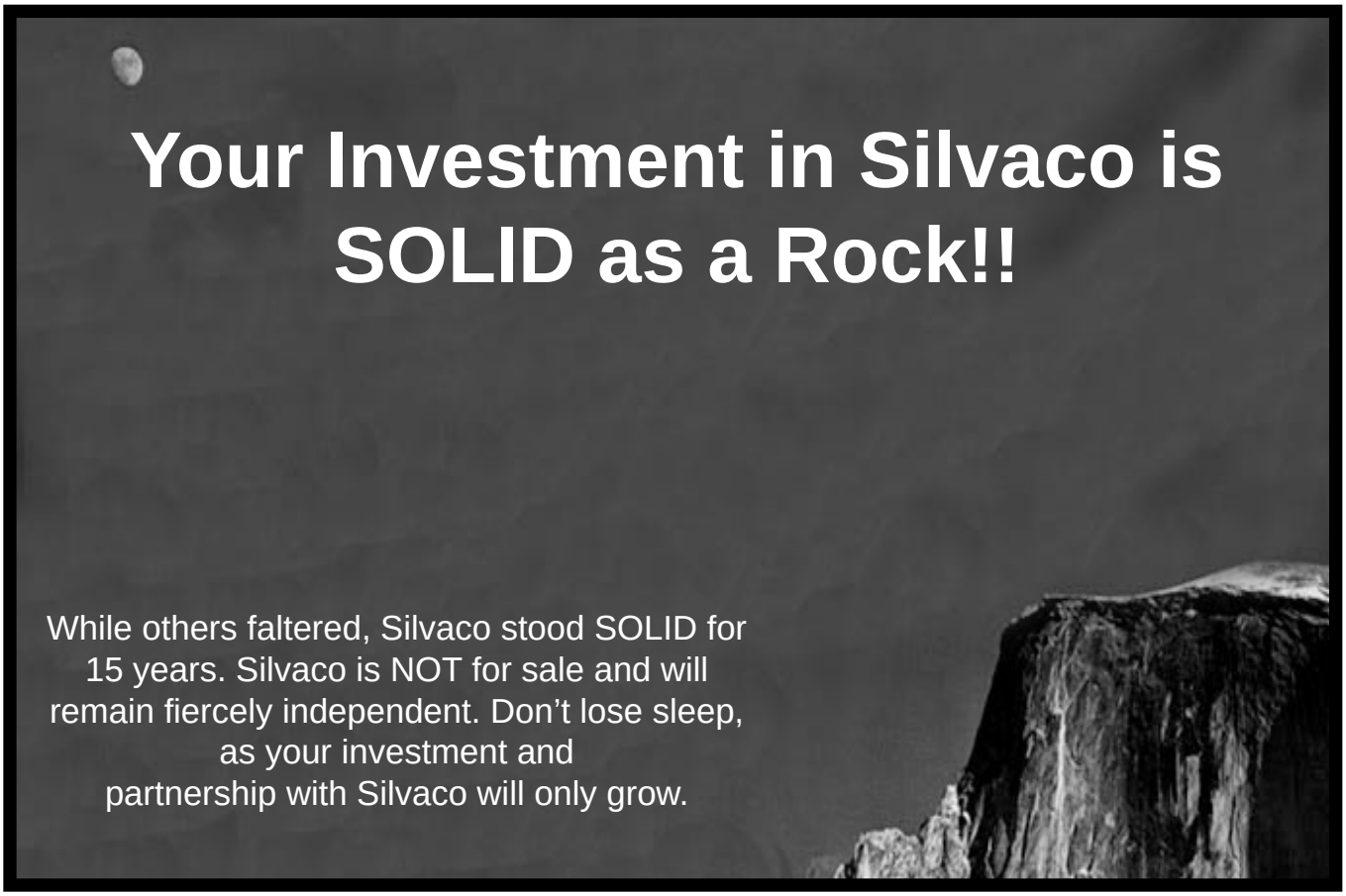

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