Simulation Standard

TCAD Driven CAD

A Journal for Process and Device Engineers

Generating a Capacitance Coefficient Database for any Chip Level LPE Tool Using *EXACT*

1.0 Introduction

EXACT is a sophisticated interconnect characterization tool integrated into the ***DISCOVERY*** framework. It is designed to build the capacitance coefficient database required by any Layout Parasitic Extraction (LPE) tool. To calculate these coefficients accurately, an internal 3D process simulator creates test structures, such as shown in Figure 1. Then an integrated 3D field solver calculates the capacitance for each device layer and test structure combination. A simple internal script language then reformats the capacitance database so that it can be used with *any* chip level LPE tool.

This article is split into two sections. The first section describes the general program operation used for ***EXACT*** and the second section in a later issue of the *Simulation Standard* will describe examples of it's use.

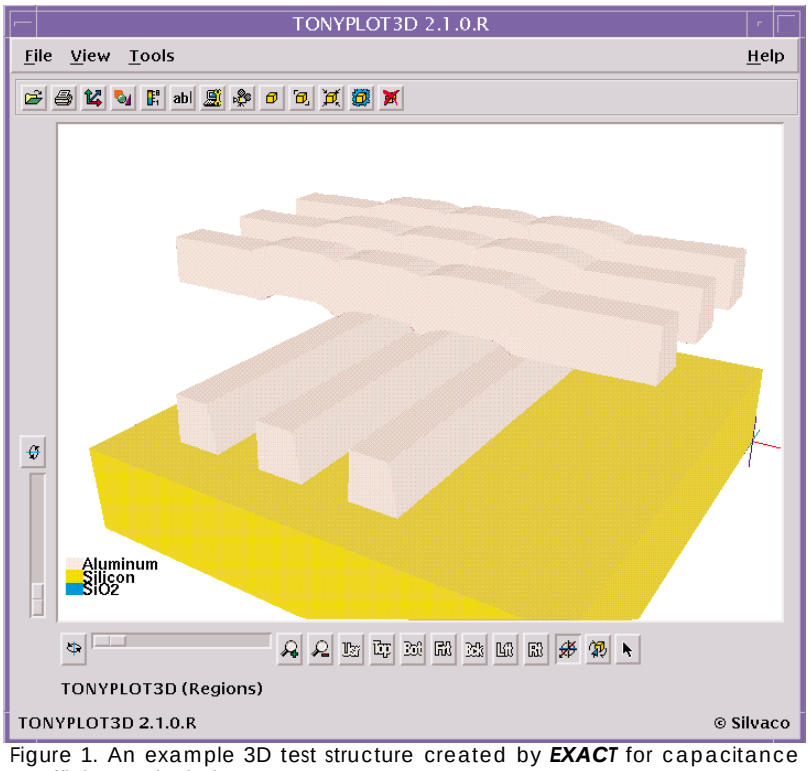

Figure 1. An example 3D test structure created by ***EXACT*** for capacitance coefficient calculations.

1.1 Why Is There A Need To Accurately Model Interconnects?

For large geometry device designs, the circuit timing delays are primarily due to the active devices. In other words, for large geometry designs, if the switching speed of the active devices is improved, the circuit delays are also improved. This situation, however, is not the case for sub-micron designs. As the technology geometry size shrinks parasitic delays from the interconnect dominate the delays originating from the active devices.

It is no coincidence that a large research effort has been directed towards researching new ways of reducing inter-connect capacitance, such as using copper and LoK materials. In today's technology, interconnect capacitance parasitics are limiting improvements gained by advances in active device design and packing density.

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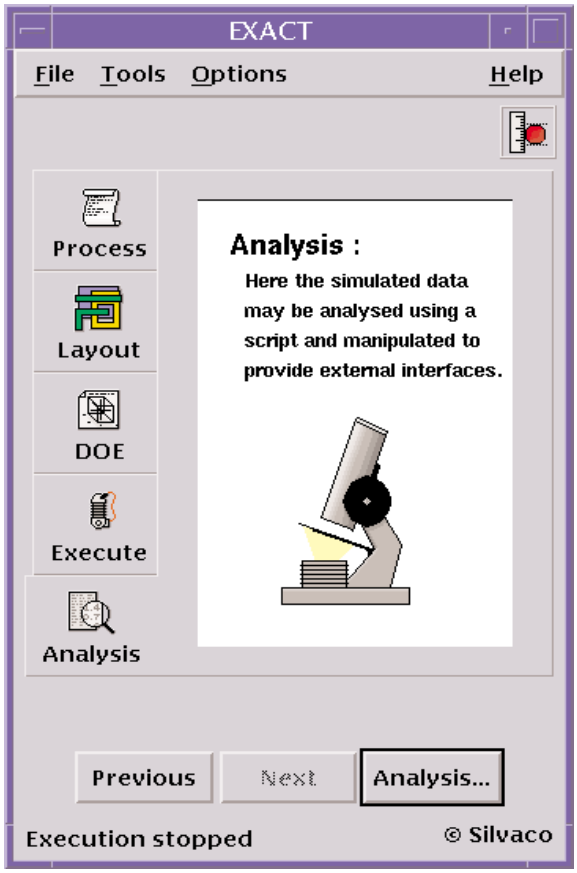

Figure 2. Exact Main GUI Showing the Five Experimental Steps

What is required is a new tool to accurately model interconnect geometry using 3D processing and a physics based 3D field solver that can be used in the inter-connect optimization process, to simulate trial and error iterations in connectivity designs, *both* for Layout and Process improvements. A tool that is easy to use and can be interfaced to existing LPE software to greatly speed up the learning curve and reduce experiments to a few days. ***EXACT*** provides these capabilities.

1.2 What Is Wrong With Capacitance Information Provided By The Foundry?

Seasoned users of full chip Layer Parasitic Extract (LPE) tools will be aware that the parasitic capacitance information provided by most foundries, although accurate, is usually very limited in nature. Often the inter- and intra-layer interconnect capacitance is provided for each layer for lines of minimum width and minimum spacing only. It would be an unusual design that only consisted of conducting lines of minimum width and minimum spacing. If any lines were not of minimum width and minimum spacing on the chip, the full chip LPE tool has to guess what the capacitance should be or ignore it altogether. This can lead to significant inaccuracies in the extracted parasitics which inevitably leads to inaccuracies in chip timing predictions.

Using ***EXACT***, the design engineer can now calculate the capacitance between lines for any width and any spacing and for any process variation between any combination of layers. The capacitance database available to the full chip LPE tool can be as complete as the user wishes it to be. Greater accuracy and predictability is the result. It is now possible to investigate the effect of different design and process philosophies in software, thus greatly improving the time taken to optimize circuit design and time to market of the product.

The limited measured data from the fabrication house can be utilized to double check the accuracy of the predictions from ***EXACT***.

2.0 EXACT Capabilities

EXACT is a flexible tool that can perform a large matrix of experiments accessible from a user friendly Graphical User Interface (GUI). The Design Of Experiments (DOE) can consist of any mix of process and layout variables. Variables such as etched sidewall angle, stepper optical source wavelength, film deposition isotrophy, insulator permittivity, multiple non planer insulator structures

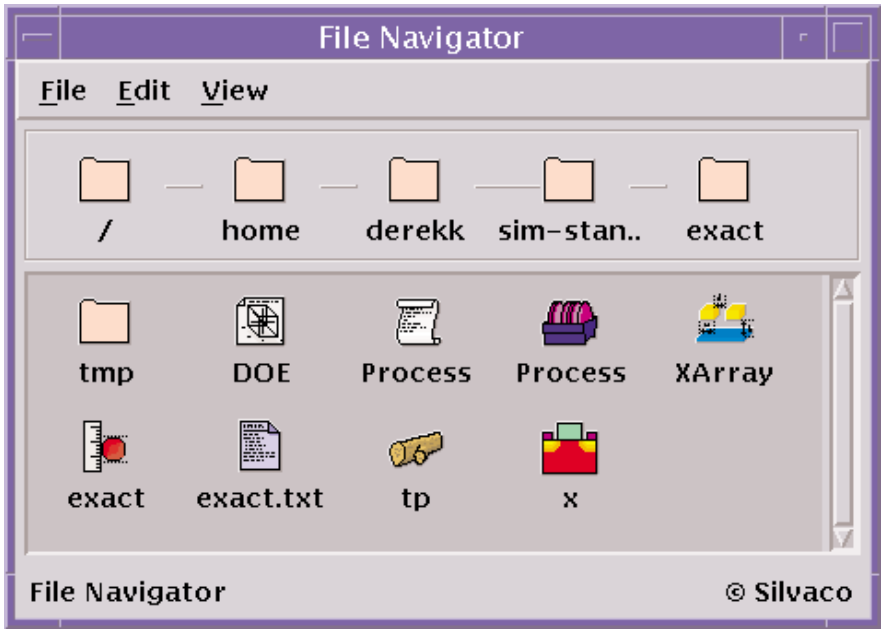

Figure 3. Exact "Matching Icon" Drag and Drop File Manager

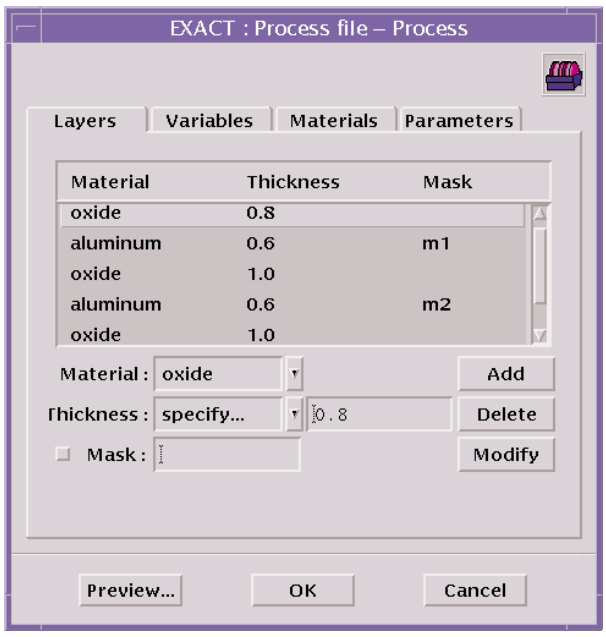

Figure 4. The Standard Mode Interactive GUI for Input of Layer Properties

layers, insulator thicknesses and general line width and spacings can all be incorporated into a single or multiple large Design Of Experiments (DOE) which typically consists of several thousand individual experiments.

The processing options in ***EXACT*** are geometric etches and depositions, or realistic etching and deposition. An integral optical solver allows photolithography effects to be taken into account, together with the exposure level at which the photoresist will develop. All relevant properties of the realistic etching, deposition and optolithographic models are user definable, including the degree of isotropy of an etch or deposition, the wavelength, aperture and shape of the exposure source, the critical intensity at which the photoresist will develop.

Users of a pre-optimized foundry process will usually have a design of experiments (DOE) that would consist of layout variables such as width and spacing. Once a technology has been fully characterized, the created data base can be used with *any* full chip LPE tool by manipulating the data base with a simple but powerful script language. The script language enables the user to write a complete LPE rule file. The script language can output text, manipulate rows and columns of the database, delete, add or modify rows and columns and fit the data to user specified formula, output the data as an LPE rule file or in graphical, Excel or text table format. This ensures that ***EXACT*** is future proof for any new chip level LPE tool that comes on the market.

3.0 Using EXACT

When starting ***EXACT*** presents the user with a intuitive Graphical User Interface (GUI) as shown in Figure 2. The main GUI provides the user with five main folders corresponding to the five distinct stages of generating a database.

The five stages are:

Stage 1: Process Information - Layer thicknesses and film properties

Stage 2: Choosing test structures - Layouts & layer combinations required

Stage 3: Design of Experiments - setting chosen variable values

Stage 4: Execute the calculations

Stage 5: Analyze, manipulate and visualize the generated database

Each stage of the procedure has a corresponding icon which opens the relevant GUI for that particular section of the experiment. The whole ***EXACT*** experiment or

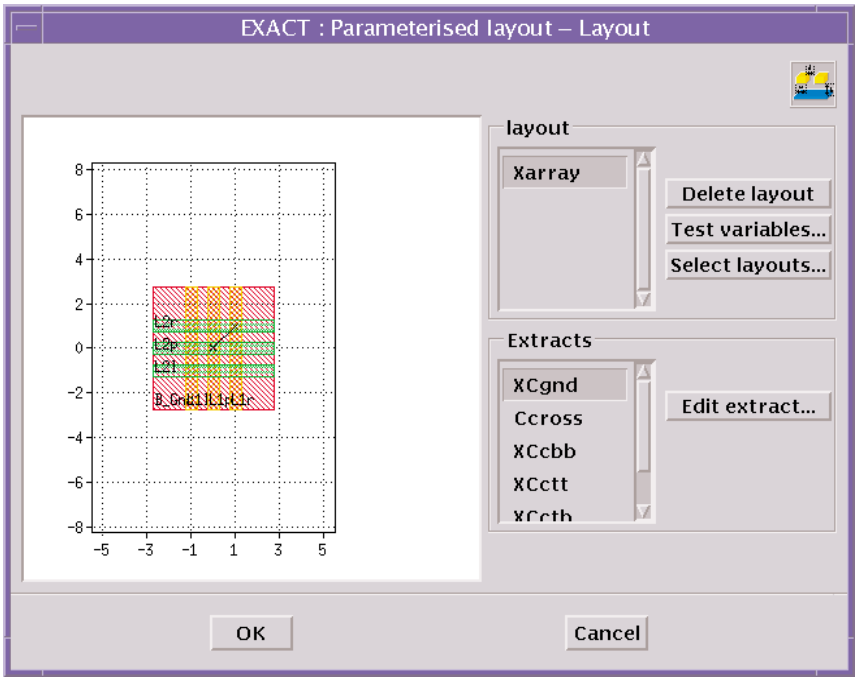

Figure 5. The Layout GUI, Showing a Typical, Pre-defined Standard Test Layout

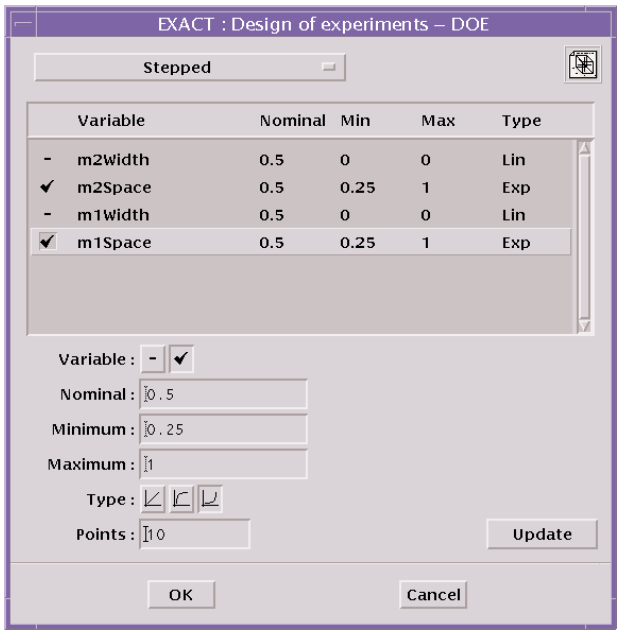

Figure 6. The design of experiments GUI, showing selection options for metal width and space.

any individual stage of the experiment, can be saved or loaded from the "drag and drop" style file manager which displays the files as icons that match the icon representing any individual stage as shown in Figure 3.

EXACT has two modes of operation, standard and advanced. In standard mode, Interactive menus create the required files or pre-defined files are simply loaded via the "drag and drop" file manager facility. In advanced mode, the user has access to the files created and can modify them using the ***EXACT*** or any other text editor. Advanced mode also offers structure layout modification or creation facilities not available in standard mode. The user can switch between standard and advanced mode at any stage of the experiment.

Process Definition

The following GUI examples are using standard mode operation. The process GUI allows simple interactive input of layer thickness, material properties and parameters that are required to be variable. Each subject is brought to the foreground by clicking on the relevant folder heading as shown in Figure 4.

Test Structure Definition

Once the device layers have been defined, the mask layout designs of the required test structures are chosen using the Layout GUI as shown in Figure 5.

The number of test structure types required depends on the complexity of the device models. For example, a reasonably accurate device model can be obtained with just two test structure types which allow extraction of overlap capacitance, layer to layer fringing capacitance and same layer fringe capacitance for any layer combinations and any space and width combinations.

The versatility of the program results from the parameterization of each test structure layout. The test structure dimensions are not defined as constants but as variables. Thus, in the interactive GUI, you can use the same base test structure layout but vary the spacing and widths in the structure. The test structure can also be defined in any combination of the layers using the interactive GUI interface. It is possible to design a comprehensive design of experiments encompassing every possible variation of line width, spacing and layer combination with a few entries in the interactive GUI.

Design of Experiment

Users do not have to enter every spacing or width you require. Simply enter the initial value, final value, number of points and how you wish to space these experimental points (either linearly, logarithmically or exponentially) as shown in figure 6.

The user can control running the experiments from the Execution control window, shown in Figure 7.

Analysis and LPE interface

On completion of all the experiments, the analysis window is displayed as shown in Figure 8. In standard mode, the user can “drag and drop” a standard script

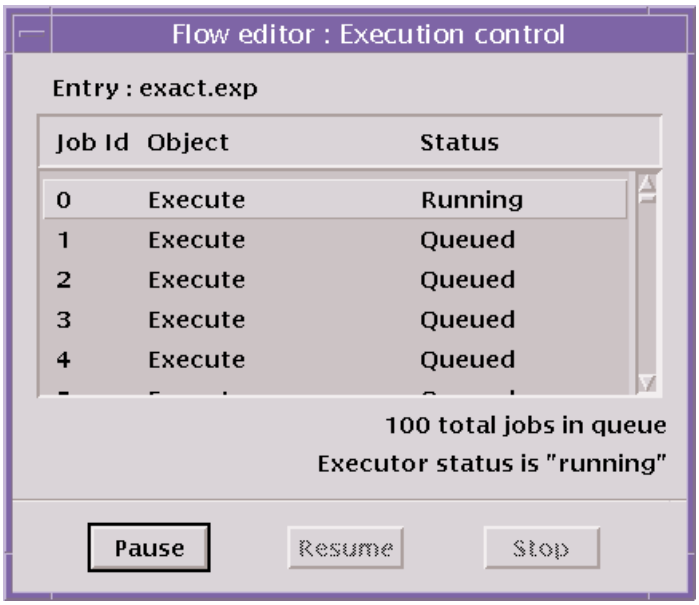

Figure 7. The Exact Runtime Window is updated in real time.

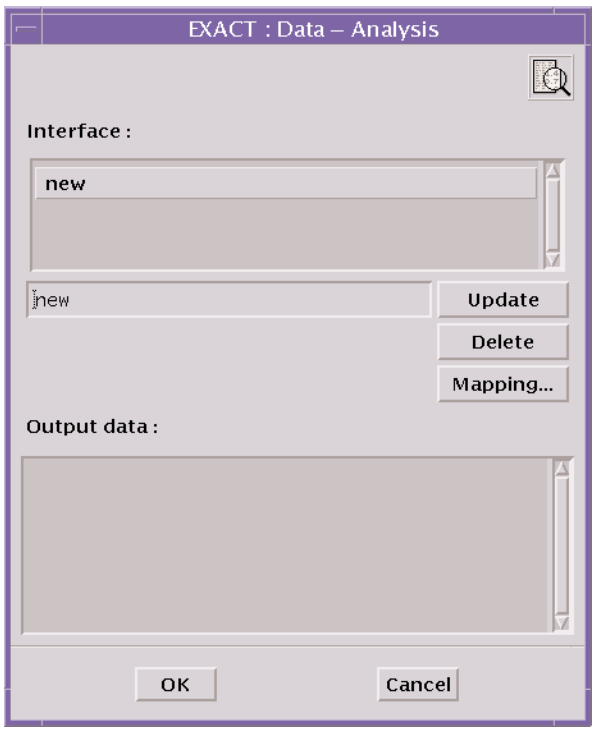

Figure 8. The Analysis Window allows multiple types of export of capacitance data.

nential spacing option discussed above. The exponential option uses smaller steps near the minimum geometry for greater accuracy where the parasitic capacitance is greatest.

More details on ***EXACT*** database manipulation using the provided script language is the subject of the next Simulation Standard article in the following issue.

4.0 Conclusion.

EXACT provides a simple way to create a comprehensive and accurate interconnect parasitic capacitance database. ***EXACT*** creates the database using a 3D process simulator and 3D field solver in a self-contained package. The creation of a comprehensive database increases the accuracy of the full chip LPE tool that is used to extract circuit parasitics. ***EXACT*** can be used with *any* LPE tool using the script language or the ready made conversion scripts provided. There are no limits on the process complexity of test structures allowed in. ***EXACT*** can account for complex non planar processing and unusual or special structures in the chip layout.

to create the active section of a full chip LPE rule file. In advanced mode an ***EXACT*** text editor is displayed which allows modification or creation of a script to act on the calculated data base. In its simplest form, an advanced script could consist of a single line to dump the database into a text table. The script file to do this would be:

```
dump @file=<filename>
@format=table
```

If the user wished to look at and manipulate the data in Microsoft's Excel, the script file would be simply:

```
dump @file=<filename>
@format=csv
```

Figure 9 shows an output using the graphical format plotted using ***TonyPlot***. The plot is a result of changing the spacing of the bottom metal stripes of the test structure shown in Figure 1 from 0.25µm to 1.0µm in 20 steps using the expo-

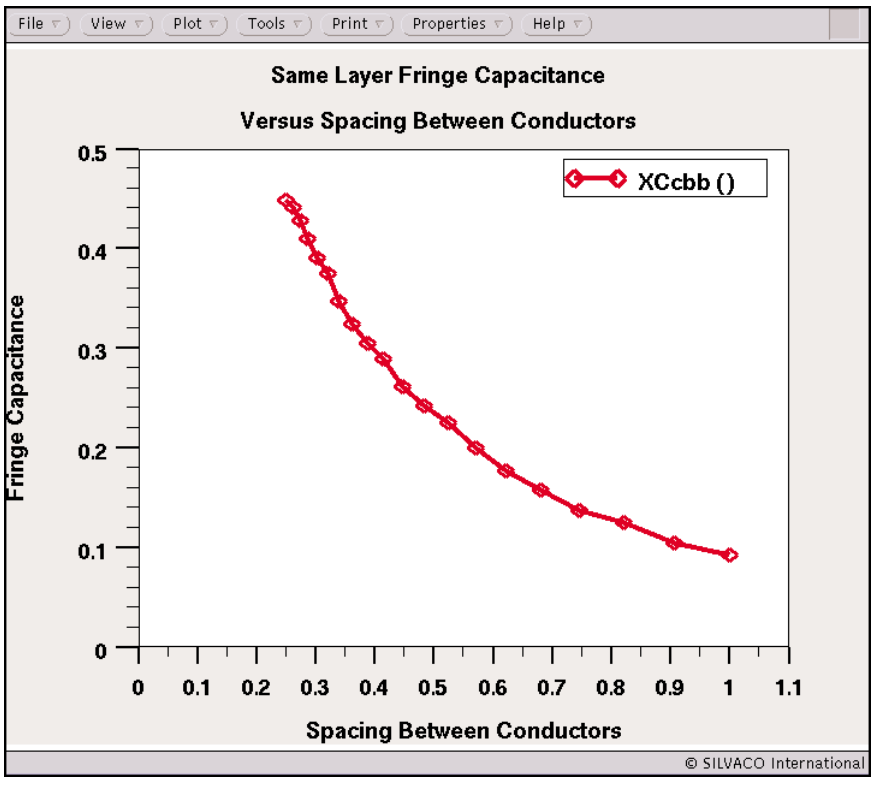

Figure 9. Same Layer Fringing Capacitance versus Line Spacing .