Simulation Standard

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A Journal for Circuit Simulation and SPICE Modeling Engineers

Intrinsic Capacitance Parameter Extraction in UTMOST III

Introduction

The intrinsic capacitance parameter extraction routine (INTCAP) is in the CAP analysis section of the ***UTMOST III*** MOS module (Routine#67). The INTCAP routine has 5 different intrinsic cap measurements and a "simulation only" capability for all intrinsic caps. Recent developments have improved the INTCAP routine. Users should have ***UTMOST III*** MOS module version 15.2.0 or higher to be able use the examples and explanations presented in this article. The INTCAP routine allows users to measure the MOS capacitances when the device is under DC bias and conducting current.

INTCAP Routine Settings

The intrinsic caps which can be measured using the INTCAP routine are:

CGD, CGS, CGC, CGB and CGG.

The user should select the proper cap using the "Multiple Selection" button located in the "Routine Control" screen for the INTCAP routine. The routine control screen can be opened from the main ***UTMOST*** screen.

The selected cap buttons will appear in red. It is recommended to select one cap at a time for the measurements until the user is familiar with the entire routine.

CGS (Gate to Source Capacitance)

Hardware Connection:

Drain -> DC analyzer (Drain terminal)

Gate -> LCR meter (Low)

Source -> LCR meter (High) AND DC analyzer (Source terminal)

Bulk -> DC analyzer (Bulk terminal)

Operation Principals

The LCR meter will supply the SOURCE Voltage. The DC analyzer SOURCE terminal is also connected to the MOS device SOURCE terminal. However the DC analyzer SOURCE terminal will work as a Voltmeter monitoring the actual SOURCE voltage of the device. The SOURCE voltage needs to be monitored because the LCR meter has an internal shunt resistor at its High terminal and the supplied voltage from the LCR meter and the actual SOURCE voltage are different due to the voltage drop across the LCR meter's shunt resistor. The measured SOURCE Voltage is fed back to ***UTMOST*** and ***UTMOST*** iterates the LCR meter voltage source supply until the device SOURCE terminal reaches to the preset VDS value.

The DRAIN terminal of the MOS device is connected to a voltage supply using the DC analyzer. The DRAIN terminal voltage is stepped to provide the initial VDS voltage before the SOURCE voltage iterations start.

The SOURCE will be stepped to provide the actual VGS voltage steps.

The GATE will be grounded by connecting it to the Low terminal of the LCR meter.

Example:

Conditions: V_{GS}=2V, V_{DS}=1V

Initially the SOURCE voltage (using the LCR meter) is set to -2V to provide VGS=2V. (GATE is grounded)

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The DRAIN voltage (Using the DC analyzer) is set to -1V to provide VDS = -1 - (-2) = 1V.

The MOS device will start conducting some current and there will be a voltage drop at the High terminal of the LCR meter which is connected to the SOURCE. The actual VDS will be different than the preset 1V. The iteration algorithm in ***UTMOST*** will start adjusting the LCR meter voltage supply to provide V_{DS}=1V and V_{GS}=2V.

The monitoring and readjusting of the LCR meter's voltage source is a slow process. During the voltage iterations the actual SOURCE voltage will be displayed on the ***UTMOST*** graphics screen. There is a current limit for each LCR meter. The user should not bias the MOS device to conduct currents which exceeds this limit. During the DC biasing of the device the DC analyzer will be in user mode.

UTMOST Measurement Setup:

V_strt_cgs/d : 0 (vds start voltage)

V_stop_cgs/d : 3 or 5 or 10 (vds stop voltage, can be different based on breakdown).

sweep_points : 15 (# of points used for vds sweep)

VG_start : 0 (vgs start voltage, should be "0" always)

VG_step : 1 (vgs step voltage)

step_points : 4 (# of vgs step)

The remaining "Measurement Variables" are not used for the CGS measurement.

Parameter Extraction

The CGS measurement will produce CGS vs. VDS curves for different step voltages of VGS. The first step curve for VGS = 0V is equivalent of overlap cap measurement curve. The Gate to Source overlap capacitance in BSIM3v3model has 3 components: CGSL + CGSO + CF

CGSL : The overlap cap for the lightly doped region of SOURCE junction.

CGSO : The overlap cap for the heavily doped region of SOURCE junction

CF : The fringing capacitance. If not given it is calculated.

The CGSL is a non-linear overlap capacitance and parameter CKAPPA is used in the overlap cap formula to describe the VGS dependency of CGSL.

The INTCAP routine will extract the CGSO, CGSL and CKAPPA parameters. Press the fit button from the options menu to perform the extraction.

Simulation and Opitimization

The INTCAP routine uses the EXTERNAL SPICE option as a simulator. ***SmartSpice*** is used to simulate the Intrinsic caps.

The CGSO and CGSL can be optimized for the VGS=0V curve. The Initial CKAPPA value can also be optimized using the remaining curves. However since CKAPPA is used for both CGDL and CGSL equations it is better to optimize this parameter using the CGC data (CGC : Gate to channel cap. CGC is the sum of CGD and CGS)

The CLC (Constant term for the short channel Cap model) and CLE (Exponential term for the short channel Cap model) can be optimized using the data other than VGS=0.

CGD (Gate to Drain Capacitance)

Hardware Connection:

Drain -> LCR meter (High) AND DC analyzer (Drain terminal)

Gate -> LCR meter (Low)

Source -> DC analyzer (Source terminal)

Bulk -> DC analyzer (Bulk terminal)

Operation Principles:

The LCR meter will supply the DRAIN Voltage. The DC analyzer DRAIN terminal is also connected to the MOS device DRAIN terminal. However the DC analyzer DRAIN terminal will work as a Voltmeter monitoring the actual DRAIN voltage of the device. The DRAIN voltage needs to be monitored because the LCR meter has an internal shunt resistor at its High terminal and the supplied voltage from the LCR meter and the actual DRAIN voltage are different due to the voltage drop accurs the LCR meter's shunt resistor. The measured DRAIN Voltage is fed back to ***UTMOST*** and ***UTMOST*** iterates the LCR meter's voltage source until the device DRAIN terminal reaches to the preset VDS value.

The SOURCE terminal of the MOS device is connected to a voltage supply using the DC analyzer. The SOURCE terminal voltage is stepped to provide the VGS values.

The SOURCE will be stepped to provide the actual VGS voltage steps.

The GATE will be grounded by connecting it to the LCR meter's Low terminal.

Example:

Conditions: V_{GS}=2V V_{DS}=1V

Initially the SOURCE voltage (using the DC analyzer) is set to -2V to provide V_{GS}=2V. (GATE is grounded)

The DRAIN voltage (Using the LCR meter) is set to -1V to provide V_{DS} = -1 - (-2) = 1V.

The MOS device will start conducting some current and

there will be some voltage drop at the High terminal of the LCR meter which is connected to the DRAIN. The actual V_{DS} will be different than the preset 1V. The iteration algorithm in ***UTMOST*** will start adjusting the LCR meter's voltage supply to provide V_{DS}=1V and V_{GS}=2V.

The monitoring and readjusting the LCR meter's voltage source is a slow slow process. During the voltage iterations the actual SOURCE voltage will be displayed on the ***UTMOST*** graphics screen.

There is a current limit for each LCR meter. The user should not bias the MOS device to conduct currents which exceeds this limit.

During the DC biasing of the device the DC analyzer will be in user mode.

UTMOST Measurement Setup:

V_strt_cgs/d : 0 (vds start voltage)

V_stop_cgs/d : 3 or 5 or 10 (vds stop voltage, can be different based on breakdown).

sweep_points : 15 (# of points used for vds sweep)

VG_start : 0 (vgs start voltage, should be "0" always)

VG_step : 1 (vgs step voltage)

step_points : 4 (# of vgs step)

The remaining "Measurement Variables" are not used for the CGD measurement.

Parameter Extraction

The CGD measurement will produce CGD vs. VDS curves for different step voltages of VGS. The first step curve for VGS = 0V is equivalent of overlap cap measurement curve. The Gate to Drain overlap capacitance in BSIM3v3model has 3 components: CGDL + CGDO + CF

CGDL : The overlap cap for the lightly doped region of DRAIN junction.

CGDO : The overlap cap for the heavily doped region of DRAIN junction

CF : The fringing capacitance. If not given it is calculated.

The CGDL is a non-linear overlap capacitance and parameter CKAPPA is used in the overlap cap formula to describe the VGS dependency of CGDL.

The INTCAP routine will extract the CGDO, CGDL and CKAPPA parameters (Press the fit button from the options menu to perform the extraction).

Simulation and Optimization

The INTCAP routine uses the EXTERNAL SPICE option as a simulator. ***SmartSpice*** is used to simulate the Intrinsic caps.

The CGDO and CGDL can be optimized for the VGS=0V curve the Initial CKAPPA value can also be optimized using the remaining curves. However since CKAPPA is used for both CGDL and CGSL equations it is better to optimize this parameter using the CGC data (CGC : Gate to channel cap. CGC is the sum of CGD and CGS).

The CLC (Constant term for the short channel Cap model) and CLE (Exponential term for the short channel Cap model) can be optimized using the data other than VGS=0.

CGC (Gate to Channel Capacitance)

Hardware Connection

Drain -> Drain and Source are shorted AND connected to LCR meter (Low)

Gate -> LCR meter (High)

Source -> Drain and Source are shorted AND connected to LCR meter (Low)

Bulk -> DC analyzer (Bulk terminal)

Operation Principles:

The LCR meter's high terminal is connected to the GATE of the MOS device. The SOURCE and DRAIN are shorted and connected to the LCR meter's Low terminal. Therefore the DRAIN and SOURCE will always be grounded. The BULK is connected to DC analyzer and its voltage is stepped. The GATE voltage will be swept and CGC will be measured for different VBS voltages. There is no need for Voltage Monitoring for the CGC measurement. Therefore CGC measurement is much faster compared to CGD or CGS measurements.

During the DC biasing of the device (Bulk terminal only) the DC analyzer will be in user mode.

UTMOST Measurement Setup:

VB_start_cgc : 0 (vbs start voltage)

VB_step_cgc : -1 (vbs stop voltage, can be different based on breakdown).

#of_step_cgc : 3 (# of vbs steps)

c_start_bias : -5 (vgs start voltage,LCR meter)

c_stop_bias : 5 (vgs stop voltage, LCR meter)

c_step_bias : 0.1 (vgs step voltage, LCR meter)

The remaining "Measurement Variables" are not used for the CGC measurement.

Parameter Extraction

The CGC measurement will produce CGC vs. VGS curves for different step voltages of VBS. No fitting operation is performed on the CGC data.

Simulation and Optimization

The INTCAP routine uses the EXTERNAL SPICE option as a simulator. ***SmartSpice*** is used to simulate the Intrinsic caps.

The CGDO, CGSO, CGDL, CGSL and CKAPPA can be optimized using the lower cap values portion of the curve. The parameter DLC (channel length reduction on one side for CV model; same as LINT but used for capacitance equations only)can be optimized using the higher cap values portion of the curve.

CGB (Gate to Channel Capacitance)

Hardware Connection:

Drain -> Drain and Source are shorted and connected to DC analyzer(Drain terminal)

Gate -> LCR meter (High)

Source -> Drain and Source are shorted and connected to DC analyzer(Drain terminal)

Bulk -> LCR meter (Low)

Operation Principles:

The LCR meter's High terminal is connected to the GATE of the MOS device.

The BULK is connected to the LCR meter's Low terminal (grounded).

The DRAIN and SOURCE are shorted and connected to the drain terminal of the DC analyzer.The drain terminal voltage will be stepped. This means both VD and VS voltages are stepped together.

The GATE voltage will be swept and CGB will be measured for different VD & VS voltages. There is no need for Voltage Monitoring for the CGB measurement. Therefore CGB measurement is much faster compared to CGD or CGS measurements.

During the DC biasing of the device (Drain terminal only) the DC analyzer will be in user mode.

UTMOST Measurement Setup:

VD_start_cgb : 0 (vd & vs start voltage)

VD_step_cgb : 1 (vd & vs stop voltage, can be different based on breakdown).

#of_step_cgb : 3 (# of vd & vs steps)

c_start_bias : -5 (vgb start voltage,LCR meter)

c_stop_bias : 5 (vgb stop voltage, LCR meter)

c_step_bias : 0.1 (vgb step voltage, LCR meter)

The remaining "Measurement Variables" are not used for the CGB measurement.

Parameter Extraction

The CGB measurement will produce CGB vs. VGB curves for different step voltages of VD & VS. No fitting operation is performed on the CGB data.

Simulation and Optimization

The INTCAP routine uses the EXTERNAL SPICE option as a simulator. ***SmartSpice*** is used to simulate the Intrinsic caps. This data is used to verify previously extracted parameters.

CGG (Total Gate Capacitance)

Hardware Connection:

Drain -> Drain, Source, Bulk are shorted and connected to LCR meter (Low)

Gate -> LCR meter (High)

Source -> Drain, Source, Bulk are shorted and connected to LCR meter (Low)

Bulk -> Drain, Source, Bulk are shorted and connected to LCR meter (Low)

The DC analyzer is not used for CGG measurement

Operation Principles:

The LCR meter's High terminal is connected to the GATE of the MOS device.

The DRAIN, SOURCE and BULK are shorted and connected to the LCR meter's Low terminal (grounded).

The GATE voltage will be swept and CGG will be measured. This is a single curve measurement. There is no additional voltage stepping and there is no need for the DC analyzer connection. CGG is a typical total Gate Capacitance measurement and it is accomplished using only the LCR meter.

UTMOST Measurement Setup:

c_start_bias : -5 (vgg start voltage,LCR meter)

c_stop_bias : 5 (vgg stop voltage, LCR meter)

c_step_bias : 0.1 (vgg step voltage, LCR meter)

The remaining "Measurement Variables" are not used for the CGG measurement.

Parameter Extraction

The CGG measurement will produce a CGG vs. VGS curve. The CGG data is used to extract the Oxide Thickness (TOX). Select the Fit option from the Options menu to execute the parameter extraction.

Simulation and Optimization

The INTCAP routine uses the EXTERNAL SPICE option as a simulator. ***SmartSpice*** is used to simulate the Intrinsic caps.

Mixed-Signal Simulation with SmartSpice in the Cadence Design Framework II

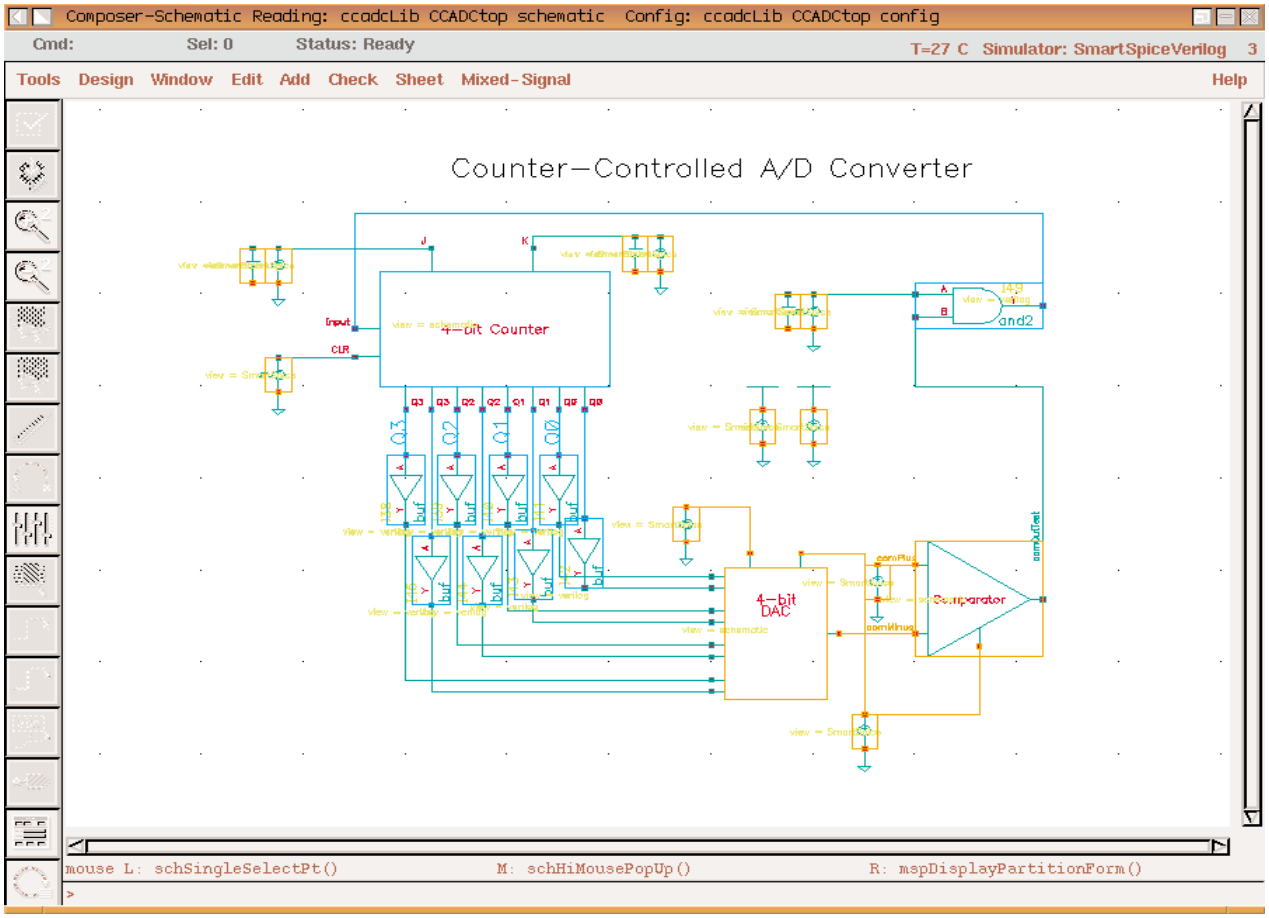

Figure 1. A successfully partitioned mixed-signal schematic.

Users of the Cadence Design Framework II (DFII, versions 4.4.0 and above) have been enjoying a tight integration between ***SmartSpice*** and the Analog Artist Electrical Design System and Composer Design Entry tools. This integration is achieved via the Cadence Spice Socket (cdsSpice) and the Open Analog Simulation Integration Socket (OASIS). It has been comprehensively documented in previous issues of the *Simulation Standard*, and also in a new application note (Ref No. SS/99-2).

The ***SmartSpice*** Interface to DFII already supports automatic netlisting, cross-probing, back-annotation and many other standard features of the DFII simulation environment. In a significant upgrade, the latest release also allows the user to make ***SmartSpice*** the analog component of their DFII mixed-signal design and simulation environment, with Cadence Verilog-XL supplying the digital simulation capability. The additional integration code is distributed in the form of a mixed-mode context file. A context file is compiled SKILL code, which is installed into the Cadence installation hierarchy along with the pre-existing analog context file, and many other related files, with the command:

```
smartspice -install -oasis
```

The most immediate indication of the enhanced capability provided by this new context file can be seen in the "Simulator/Directory/Host" dialog, under the "Setup" menu in Analog Artist, where both "SmartSpice" and "SmartSpiceVerilog" appear in the list of available simulators. When this latter option is selected Analog Artist is placed in mixed-signal mode, and ***SmartSpice*** becomes the controller in a master-slave relationship with Verilog-XL. All further integration is transparent to the user.

In order to support mixed-signal simulation, ***SmartSpice*** now recognizes new ".A2D" and ".D2A" cards. These cards are automatically generated by the Analog Artist netlisting process in mixed-mode operation. Although it should never be necessary for a user to manually add or edit these statements, their syntax is given here since it may be useful in understanding how the digital and analog partitions interact.

The A2D node is specified by the card:

```
.A2D Dout Ain Vlow Vhigh TX
```

with parameters:

Dout - the name of the node in the Verilog deck.

Ain - the name of the node in the ***SmartSpice*** deck.

Vlow - the upper threshold for a logic 0.

Vhigh - the lower threshold for a logic 1.

TX - the minimum length of time that a node volt age must remain between Vlow and Vhigh in order to be considered a digital "X".

The interface mechanism for analog-to-digital (A2D) nodes is that Verilog-XL simply reads the voltages directly from these nodes, and converts them to its own logic levels, using Vlow, Vhigh and TX.

The D2A node is specified by the card:

```
.D2A Din Vsrc1 <Vsrc2> Vlow Vhigh Trise Tfall
```

with parameters:

Din - the name of the digital to analog interface node.

Vsrc1 - a voltage source that controls the transitions between logic 0's and 1's.

Vsrc2 - the optional voltage source for controlling strength.

Vlow - the voltage corresponding to logic 0.

Vhigh - the voltage corresponding to logic 1.

Trise - the time to rise from logic 0 to logic 1.

Tfall - the time to fall from logic 1 to logic 0.

The interface mechanism for digital-to-analog (D2A) nodes is simply to insert extra voltage sources (and perhaps also resistors or small subcircuits: the exact details are determined by the netlisting algorithms chosen in Analog Artist) into the ***SmartSpice*** deck, at the interface nodes. By controlling these PWL voltages, Verilog-XL communicates its logic levels to ***SmartSpice***.

SmartSpice also now recognizes certain new command-line arguments, supplied by Analog Artist for the control of Verilog-XL. These command-line arguments are:

-mixmod - indicates that a mixed-signal simulation is in progress;

-slave - takes a quoted string containing command-line arguments to be passed to Verilog-XL.

-slvhost, -shellhost, -shellport - take arguments indicating which machines and ports to use.

-mmdebug - turns on certain debugging messages.

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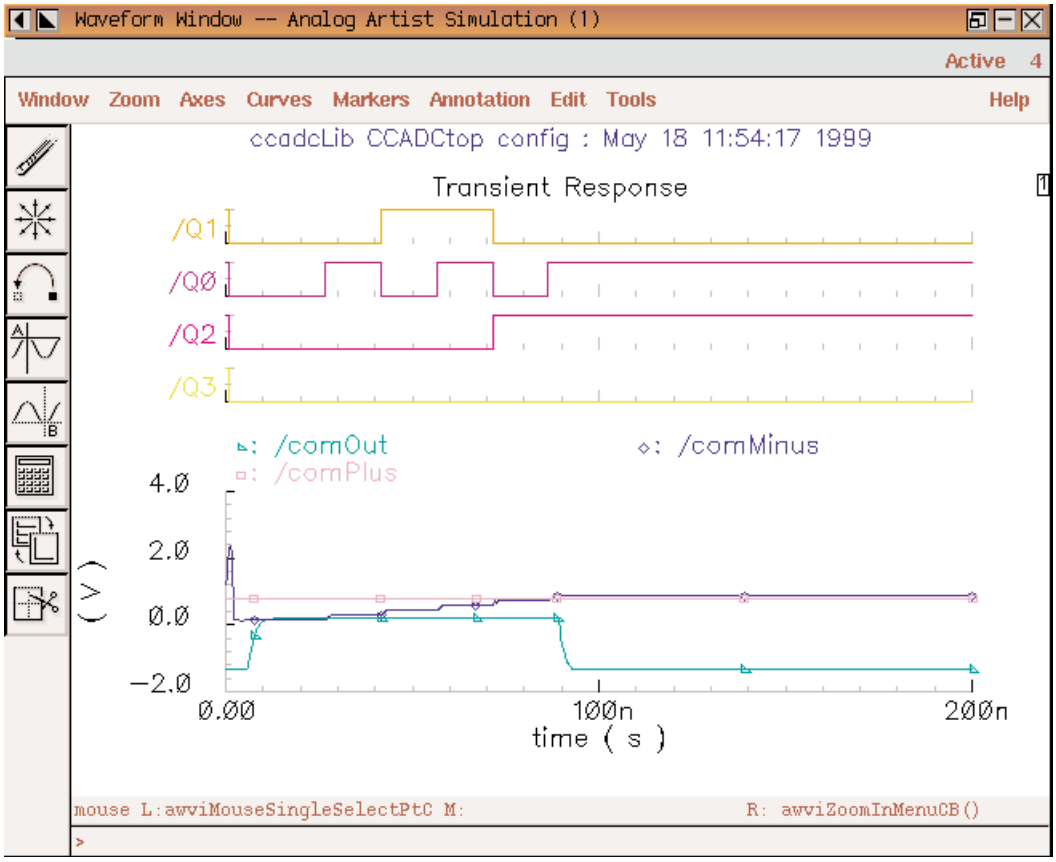

Figure 2. The waveform window, showing the results of a mixed-signal simulation.

SPAYN: Golden Device Search Algorithm, EKV MOSFET Model and Improved GUI

Introduction

The addition of important features in the latest version of ***SPAYN*** (1.7.3.R) makes it an even more useful and versatile statistical parameter and yield analysis tool. The list of spice models available in ***SPAYN*** has been expanded to include the EKV MOSFET model. The new "Golden Device" function locates the observation in a particular database that is closest to the theoretical mean observation. This "Golden Device" is then considered to be the average observation that best characterizes that database. Several new plotting symbols have been added to the scattergram plotting facility allowing a clearer graphical representation of data. It is also now possible to locate the position of the minimum or maximum record in a given database without the need to manually sort through the complete data set.

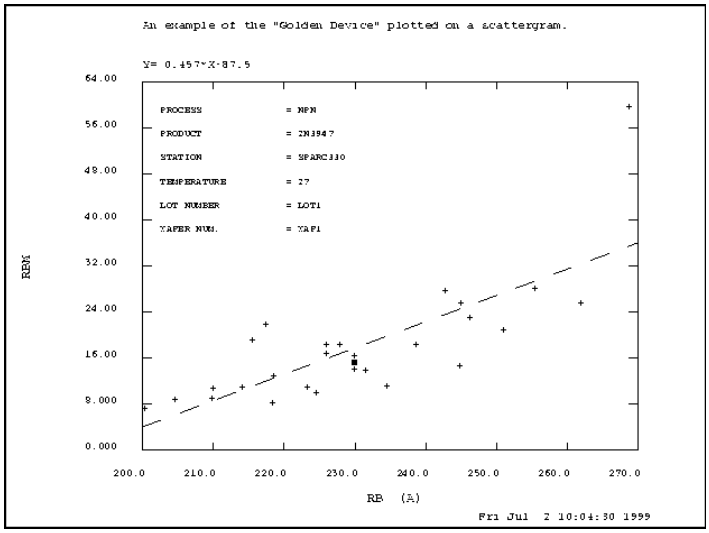

Figure 1. Scattergram: Golden device represented by a solid square

EKV MOSFET model

The EKV MOSFET model has been added to the list of device levels currently available in ***SPAYN***. An EKV SPICE model (level = 44) can be set up by selecting Setup→Spice→Edit Models from the main ***SPAYN*** window and then entering 44 for the model level. The other parameters are also selected accordingly (see [1] for more details).

Once the EKV SPICE model has been set up various device characteristics can be computed. This is accomplished by selecting Setup→Device Characteristic from the main ***SPAYN*** window. The user then selects the following options: Device Type = MOSFET, Device Level = EKV and Spice Model Setup = PMOD, where PMOD is the previously set up EKV SPICE model.

Golden Device

The Golden Device facility allows the modeling engineer to calculate which observation (or observations) in a particular database most closely match the mean, based on some dissimilarity measure. This observation or record is referred to as the "Golden Device". The name is derived from the fact that if the observations actually represent devices then the algorithm locates that measured device closest to the mean This means the measured device that *on average* best describes the given database, hence the name "Golden Device". The mean observation is constructed from individual parameter sample means and does not usually belong to the set of measured data.

In general, given a database of N measured observations or records, each described by p parameters, and a dissimilarity measure D, the algorithm [2] finds the m records closest to a query record (not necessarily in the database) with specified parameter values. The search algorithm uses the Euclidean distance, which is a special case of the Minkowski distance metric in equation (1) with $q = 2$.

$$D_{rs} = \left(\sum_{j=1}^{p} |x_{rj} - x_{sj}|^{q} \right)^{\frac{1}{q}} \qquad (1)$$

where D_{rs} is the distance between 2 records r and s and x_{rj} is the value of the j^{th} parameter for the r^{th} observation. In fact since the mean is being used, x_{sj} is replaced in equation (1) by m_j the sample mean of parameter j.

The "Golden Device" window is opened by clicking on Analysis→Golden Device from the main ***SPAYN*** window.

i. Select which parameters to include, the algorithm then uses the sample means of these parameters to locate the Golden Device i.e. the observation nearest the mean, based on the chosen dissimilarity measure.

ii. Enter the required number of neighbors (<15). The search algorithm then looks for that number of observations closest to the mean (rank 1 being the nearest). For example choosing 2 neighbors would return the two observations closest to the mean, based on the specified dissimilarity measure.

iii. Choose a distance metric (1-8), the value 2 (default) corresponds to the Euclidean distance. This is equivalent to setting q=2 in equation (1).

iv. Press "Apply" to implement the search algorithm. The observations closest the mean will be displayed in the "Observation Number(s)" window. To view the parameter values for these observations click on Data Search->Search Results from the main menu, and then select "Statistics", "View Table" or "View Parameters". It is also possible to view the "Golden Device" graphically by using the "Golden Device" toggle in the "Scattergram" window (Figure 1).

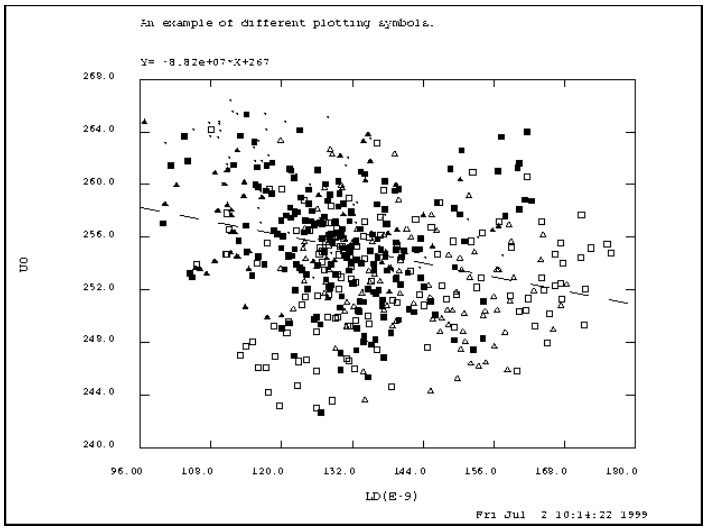

Figure 2. Scattergram: Each wafer is represented by a different plot symbol.

Scattergram Plotting Symbols

In addition to the existing scattergram plot symbols (markers), squares and triangles have also been added. Both of these symbols are available in outline or solid form e.g. ❑, Δ, ■ and ▲. The scattergram plotting symbol can be changed by selecting Setup→Plots→Scattergram Palette, from the main menu. The user can then choose the marker type (plot symbol) from the pulldown menu. It is also possible to display different attributes in a scattergram with different plotting symbols. This is achieved by selecting Setup→Plots→Highlight by Attributes, from the main window. Figure 2 shows an example where data from each wafer is represented by a different plot symbol.

Statistical Summary Parameter Information Display

One problem that occasionally confronts a modeling engineer is the necessity to locate the record in a database that corresponds to the maximum or minimum value of a particular parameter. This option is now available in ***SPAYN***, alleviating the need to sift through all the data points. In addition to providing the location of the required record, this facility also supplies attribute information for the selected parameter. It is accessed by clicking on the maximum or minimum value of a particular parameter in the "Statistical Summary" window. The "Statistical Summary" window is generated by selecting Data Search→Search Results→Statistics from the main menu. Figure 3 demonstrates the ***SPAYN*** Statistical Summary window, with the Parameter Information window inset. In this example the minimum value for the parameter U0 is located at observation / record number 539.

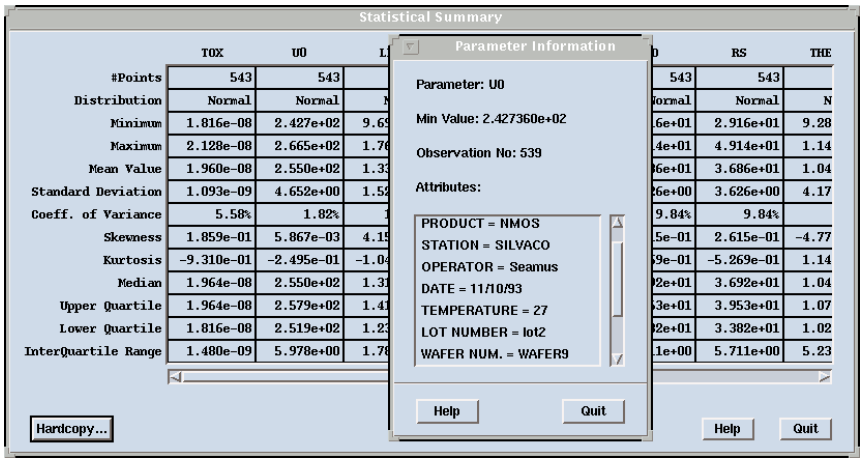

Figure 3. Parameter Information and minimum value displayed for variable UO. The minimum value is located at observation/record number 539.

References

[1] M Bucher, C Lallement, C. C Enz, and F Krummenacher. Accurate MOS Modeling for Analog CIrcuit Simulation using the EKV Model. In *Proceedings IEEE International Symposium on Circuits and Systems (ISCAS),* pages 703-706, 1996.

[2] J.H. Friedman, J. L Bentley, and R. A Finkel. An Algorithm for Finding Best Matches in Logarithmic Expected Time. *ACM Transactions on Mathematical Software,* 3:209-226, 1977.

Calendar of Events

April

1
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3
4 MRS Spring Meeting - San Francisco, CA
5 MRS Spring Meeting - San Francisco, CA
6 MRS Spring Meeting - San Francisco, CA
7 MRS Spring Meeting - San Francisco, CA
8 MRS Spring Meeting - San Francisco, CA
9 MRS Spring Meeting - San Francisco, CA
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12 Int'l Symposium on Physical Design - Monterey, CA
13 Int'l Symposium on Physical Design - Monterey, CA
14 Int'l Symposium on Physical Design - Monterey, CA
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May

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2 ECS-SOI - Seattle, WA
3 ECS-SOI - Seattle, WA
4 ECS-SOI - Seattle, WA
5 ECS-SOI - Seattle, WA
6 ECS-SOI - Seattle, WA
7 ECS-SOI - Seattle, WA
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9 Int'l Symposium on Plasma Process-Induced Damage - Monterey, CA
10 Int'l Symposium on Plasma Process-Induced Damage - Monterey, CA
11 Int'l Symposium on Plasma Process-Induced Damage - Monterey, CA
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16 CICC - San Diego, CA
17 CICC - San Diego, CA
18 CICC - San Diego, CA
19 CICC - San Diego, CA
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24 IITC '99- Burlingame, CA
25 IITC '99- Burlingame, CA
26 IITC '99- Burlingame, CA Int'l Symp. On Power Semiconductor Devices and IC's - Toronto, Canada
27 Int'l Symp. On Power Semiconductor Devices and IC's - Toronto, Canada
28 Int'l Symp. On Power Semiconductor Devices and IC's - Toronto, Canada
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Bulletin Board

Semiconductors in Seattle

The Electrochemical Society Meeting provides the perfect forum for Silvaco's leading tools. Silvaco demonstrations, engineers, and sales will be present for this May 2nd-5th conference in the Great Pacific Northwest.

Custom Integrated Success

Silvaco once again will be present at the Custom Integrated circuits Conference in San Diego. Our Southern California team of experts will be on hand to demonstrate the power of integrating Silvaco into your design process.

Connect to the Future!

The International Interconnect Technology Conference is the stage for Silvaco's world class interconnect software. This May 24th-26th event will highlight the dominance of Silvaco's interconnect platform.

For more information on any of our workshops, please check our web site at ***http://www.silvaco.com***

Hints, Tips and Solutions

Mustafa Taner, Applications and Support Engineer

Q. How can I use the SOI BSIM3_MG routine to extract inital SOI SPICE model parameters.

A. The BSIM3_MG routine in SOI module of ***UTMOST*** III can be used to extract SOI model parameters. The SOI BSIM3_MG routine operation is similar to the one in MOS module. However the "Measurement Variables" (Figure 1) and biasing of the SOI device is unique.

The SOI devices can have 4 or 5 terminals. For 4 terminal SOI devices typically the bulk node floats and drain, gate, source and backgate terminals are used for biasing. For 5 terminal SOI devices the bulk terminal has a contact too. The number of terminals for the SOI devices can be defined by toggling the "# of Terminals" button in the system screen.

In order to support the combinations of 4 or 5 terminal devices the measurement setup screen of SOI BSIM3_MG routine had to be redesigned. The SOI BSIM3_MG routine can handle stepping of bulk bias while the backgate bias is constant or stepping of back-gate bias while bulk bias is constant.

The definition of the "Measurement variables" of SOI BSIM3_MG routine:

VGS_start_vg: VGS start value for IDS/VGS curves.

VGS_stop_vg: VGS stop value for IDS/VGS curves.

VDS_low_vg: VDS constant voltage for (low bias) IDS/VGS curve.

VDS_high_vg: VDS constant voltage for (high bias) IDS/VGS curve.

VDS_start_vd: VDS start value for IDS/VDS curves.

VDS_stop_vd: VDS stop value for IDS/VDS curves.

VGS_strt1_vd: First VGS step value for IDS/VDS curve where VBS=0V. This value is automatically set by the routine. The value is based on the measured VTH of each device and the "VGS_strt_off" variable : VGS_strt1_vd = VTH + VGS_strt_off

VGS_strt2_vd: First VGS step value for IDS/VDS curve where VBS=Vbulk_vd. This value is automatically set by the routine. The value is based on the measured VTH of each device and the "VGS_strt_off" variable : VGS_strt2_vd = VTH (at VBS=Vbulk_vd) + VGS_strt_off

VGS_strt_off: Offset voltage used to define VGS_strt1_vd and VGS_strt2_vd.

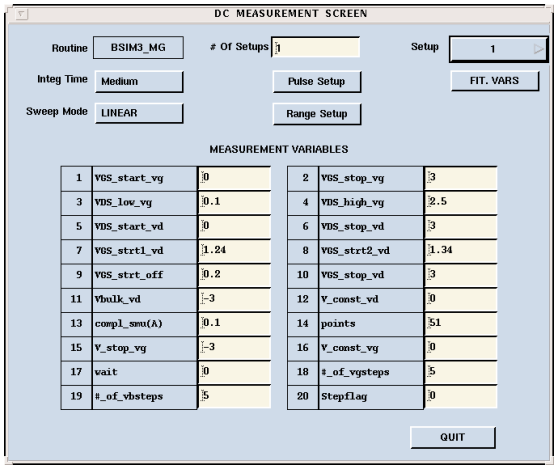


Figure 1. SOI BSIM3_MG routine measurement variables screen.

VGS_stop_vd: Maximum VGS voltage applied at IDS/VDS curves.

V_bulk_vd: If the #_of_terminals is set to 4: The voltage applied to backgate for (high bias) IDS/VDS curves.

If the #_of_terminals is set to 5 and If the step_flag is set to 0: The voltage applied to backgate for (high bias) IDS/VDS curves.

If the #_of_terminals is set to 5 and If the step_flag is set to 1: The voltage applied to body for (high bias) IDS/VDS curves.

V_const_vd: If the #_of_terminals is set to 4: V_const_vd is not used.

If the #_of_terminals is set to 5 and If the step_flag is set to 0: The voltage applied to body for all (low and high bias) IDS/VDS curves.

If the #_of_terminals is set to 5 and If the step_flag is set to 1: The voltage applied to backgate for all (low and high bias) IDS/VDS curves.

compl_smu(A): Compliance current for all SMUs.

points: Number of points for each voltage sweep.

V_stop_vg: If the #_of_terminals is set to 4: The maximum voltage applied to backgate for all IDS/VGS curves.

If the #_of_terminals is set to 5 and If the step_flag is set to 0: The maximum voltage applied to backgate for all IDS / VGS curves.

If the #_of_terminals is set to 5 and If the step_flag is set to 1: The maximum voltage applied to body for all IDS / VGS curves.

V_const_vg: If the #_of_terminals is set to 4: V_const_vg is not used.

If the #_of_terminals is set to 5 and If the step_flag is set to 0: The voltage applied to body for all IDS / VGS curves.

If the #_of_terminals is set to 5 and If the step_flag is set to 1: The voltage applied to backgate for all IDS / VGS curves.

wait: Wait time for each sweep.

#_of_vgsteps: Number of VGS steps for IDS / VDS curves.

#_of_vbsteps: Number of VBS (bulk) or VBG (backgate) steps for IDS / VGS curves.

step_flag: VBS (bulk) or VBG (backgate) stepping flag. If number of terminals is set to 4 then the step_flag is not used. The step_flag is active only for 5 terminal devices.

The data collection and extraction algorithms of SOI BSIM3_MG is same as MOS BSIM3_MG routine. Related information can be obtained from the MOS Extraction Manual Volume #1.

...continued from page 6

As ***SmartSpice*** is designed to be the master, and Verilog-XL the slave, ***SmartSpice*** is generally in control of time-stepping. The basic flow in the simulation is:

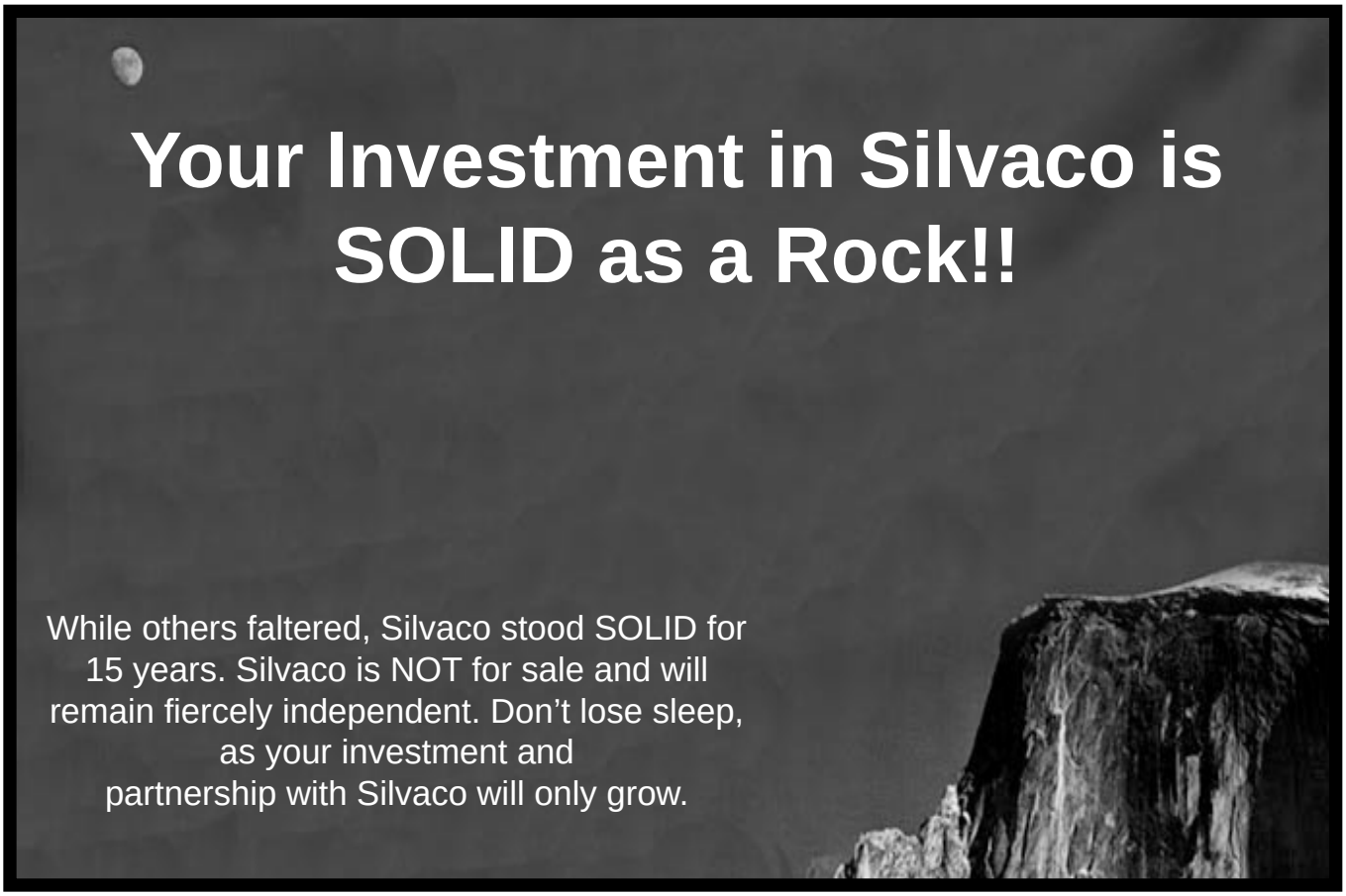
1. ***SmartSpice*** starts, and parses the input deck. If the deck contains at least one .A2D or .D2A node, and if at least one DC or transient analysis is requested, Verilog-XL is started with appropriate command-line arguments. If there are no interface nodes, or only AC analysis is requested, a regular all-analog simulation will be performed, but Verilog-XL will not be started.
2. Simulators exchange information on the size of the timestep and on interface nodes. Inconsistencies between interface-node specifications in the ***SmartSpice*** input deck and Verilog-XL input files will be flagged at this point.
3. DC analysis is performed if requested.
4. Transient analysis is performed if requested. Before committing to a particular timestep, however, ***SmartSpice*** will ask Verilog-XL whether there are any digital events occurring (at the interface nodes) within this timestep, and if so, will adjust the timestep to conform. In this way, the two simulators synchronize at all events on the interface nodes, but simulate more or less independently otherwise.
5. When all requested analyses have been performed, both **SmartSpice** and Verilog-XL will terminate.

The SmartSpice Interface to DFII includes a "SmartSpiceVerilog" template for mixed-signal hierarchy configuration; it is essential that the user select this template as the basis for any existing, or new, mixed-signal top-level cells. Once the configuration process has been completed (once, only for each design), the user should be able to successfully partition the circuit under analysis. An example of a partitioned mixed-signal schematic is shown in figure 1. This is the CCADC example, a 4-bit analog-to-digital converter, which can be found in the Cadence samples directory: the analog, digital and mixed-mode portions of this circuit are color-coded in the normal fashion.

Since ***SmartSpice*** outputs Cadence Parameter Storage Format (PSF) data files, the results of an analog simulation, or of the analog portion of a mixed-signal simulation, can be plotted in the Cadence Waveform Window, together with any digital waveforms output by Verilog-XL. The analog and digital waveforms resulting from a mixed-mode simulation of the CCADC circuit are shown in figure 2.

In order to make use of ***SmartSpice*** within the Analog Artist simulation environment, the user will have to purchase from Cadence certain license features. For loading designs into Analog Artist, prior to performing any simulations of any kind and independent of the simlutor to be used, the user will first require license feature 34510, the "Artist Design Environment", and to specifically enable access to ***SmartSpice*** through the OASIS interface, the user will additionally require license feature 32100 (symbolic name: OASIS_Simulation_Interface). Those two features are a necessary and sufficent set for the completion of strictly analog simulations via ***SmartSpice.***

In order to perform mixed-signal simulations, independent of the simulator to be used, the user will also require license feature 32140, the "Mixed-Signal Simulation Interface Option", and to actually carry out the digital portion of a mixed-signal simulation the user will require license feature 26000 (symbolic name: VERILOG-XL).



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