

Mixed-Signal Simulation with SmartSpice in the Cadence Design Framework II

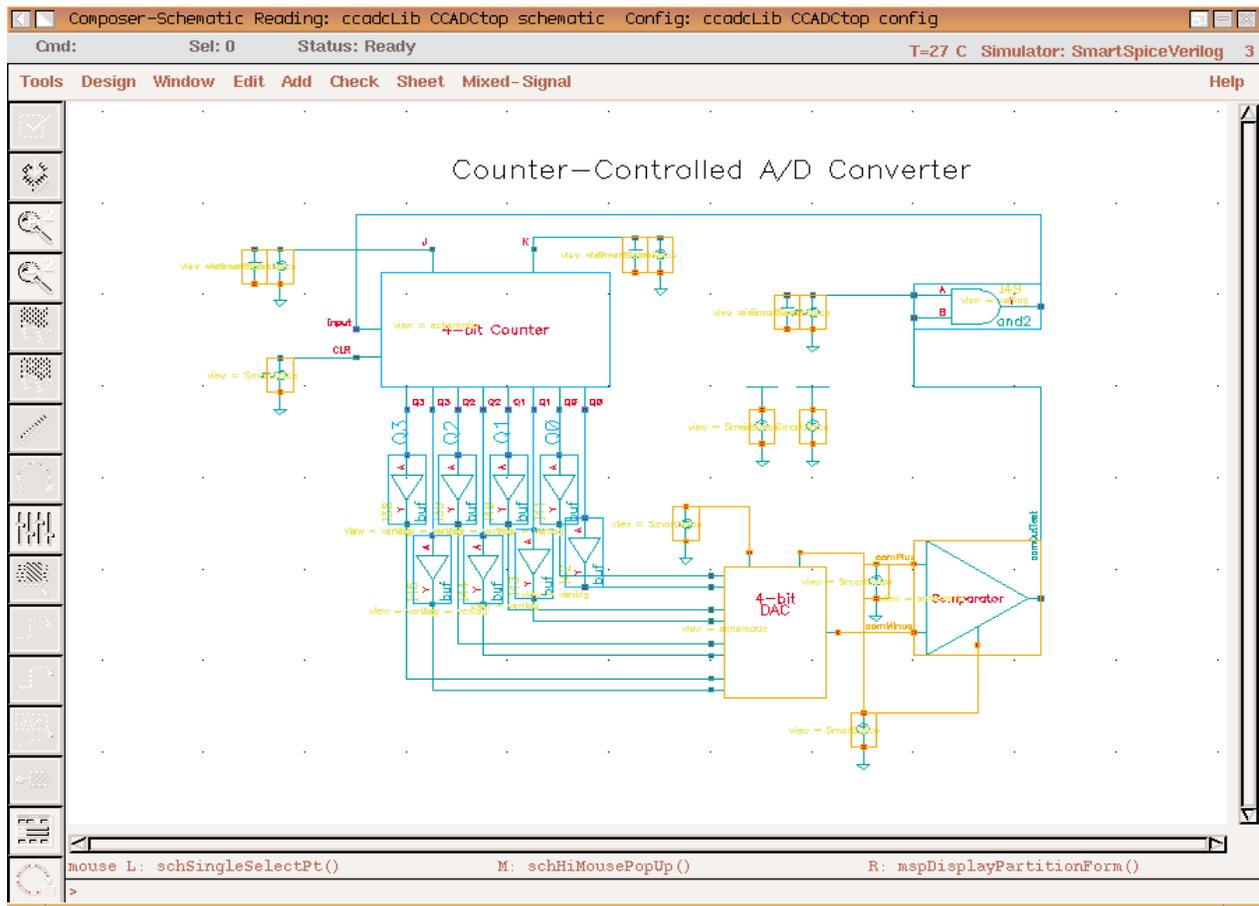


Figure 1. A successfully partitioned mixed-signal schematic.

Users of the Cadence Design Framework II (DFII, versions 4.4.0 and above) have been enjoying a tight integration between **SmartSpice** and the Analog Artist Electrical Design System and Composer Design Entry tools. This integration is achieved via the Cadence Spice Socket (cdsSpice) and the Open Analog Simulation Integration Socket (OASIS). It has been comprehensively documented in previous issues of the *Simulation Standard*, and also in a new application note (Ref No. SS/99-2).

The **SmartSpice** Interface to DFII already supports automatic netlisting, cross-probing, back-annotation and many other standard features of the DFII simulation environment. In a significant upgrade, the latest release also allows the user to make **SmartSpice** the analog component of their DFII mixed-signal design and simulation environment, with Cadence Verilog-XL supplying the digital simulation capability. The additional integration code is distributed in the form of a mixed-mode context file. A context file is compiled SKILL code, which is installed into the Cadence installation hierarchy along

with the pre-existing analog context file, and many other related files, with the command:

```
smartspice -install -oasis
```

The most immediate indication of the enhanced capability provided by this new context file can be seen in the "Simulator/Directories/Host" dialog, under the "Setup" menu in Analog Artist, where both "SmartSpice" and "SmartSpiceVerilog" appear in the list of available simulators. When this latter option is selected Analog Artist is placed in mixed-signal mode, and **SmartSpice** becomes the controller in a master-slave relationship with Verilog-XL. All further integration is transparent to the user.

In order to support mixed-signal simulation, **SmartSpice** now recognizes new ".A2D" and ".D2A" cards. These cards are automatically generated by the Analog Artist netlisting process in mixed-mode operation. Although it should never be necessary for a user to manually add or edit these statements, their syntax is given here since it may be useful in understanding how the digital and analog partitions interact.

The A2D node is specified by the card:

```
.A2D Dout Ain Vlow Vhigh TX
```

with parameters:

- Dout - the name of the node in the Verilog deck.
- Ain - the name of the node in the **SmartSpice** deck.
- Vlow - the upper threshold for a logic 0.
- Vhigh - the lower threshold for a logic 1.
- TX - the minimum length of time that a node voltage must remain between Vlow and Vhigh in order to be considered a digital "X".

The interface mechanism for analog-to-digital (A2D) nodes is that Verilog-XL simply reads the voltages directly from these nodes, and converts them to its own logic levels, using Vlow, Vhigh and TX.

The D2A node is specified by the card:

```
.D2A Din Vsrc1 <Vsrc2> Vlow Vhigh Trise Tfall
```

with parameters:

- Din - the name of the digital to analog interface node.
- Vsrc1 - a voltage source that controls the transitions between logic 0's and 1's.
- Vsrc2 - the optional voltage source for controlling strength.

Vlow - the voltage corresponding to logic 0.

Vhigh - the voltage corresponding to logic 1.

Trise - the time to rise from logic 0 to logic 1.

Tfall - the time to fall from logic 1 to logic 0.

The interface mechanism for digital-to-analog (D2A) nodes is simply to insert extra voltage sources (and perhaps also resistors or small subcircuits: the exact details are determined by the netlisting algorithms chosen in Analog Artist) into the **SmartSpice** deck, at the interface nodes. By controlling these PWL voltages, Verilog-XL communicates its logic levels to **SmartSpice**.

SmartSpice also now recognizes certain new command-line arguments, supplied by Analog Artist for the control of Verilog-XL. These command-line arguments are:

- mixmod - indicates that a mixed-signal simulation is in progress;
- slave - takes a quoted string containing command-line arguments to be passed to Verilog-XL.
- slvhost, -shellhost, -shellport - take arguments indicating which machines and ports to use.
- mmdebug - turns on certain debugging messages.

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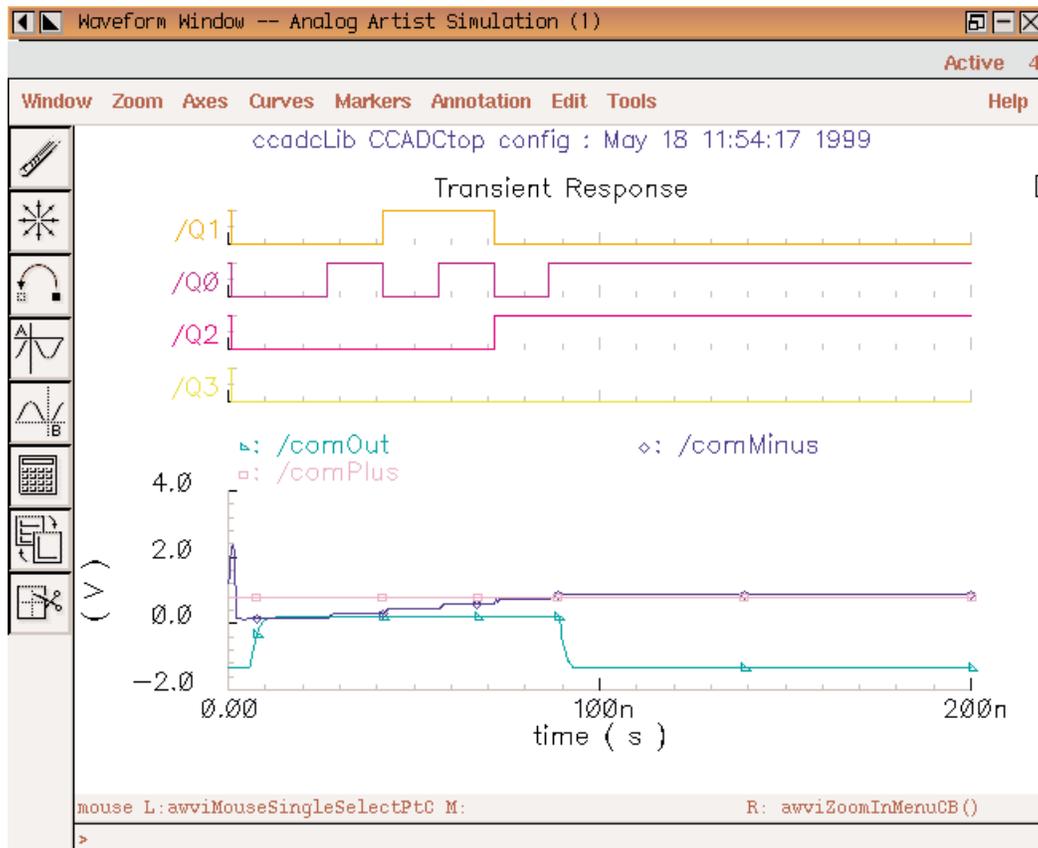


Figure 2. The waveform window, showing the results of a mixed-signal simulation.

As **SmartSpice** is designed to be the master, and Verilog-XL the slave, **SmartSpice** is generally in control of time-stepping. The basic flow in the simulation is:

1. **SmartSpice** starts, and parses the input deck. If the deck contains at least one .A2D or .D2A node, and if at least one DC or transient analysis is requested, Verilog-XL is started with appropriate command-line arguments. If there are no interface nodes, or only AC analysis is requested, a regular all-analog simulation will be performed, but Verilog-XL will not be started.
2. Simulators exchange information on the size of the timestep and on interface nodes. Inconsistencies between interface-node specifications in the **SmartSpice** input deck and Verilog-XL input files will be flagged at this point.
3. DC analysis is performed if requested.
4. Transient analysis is performed if requested. Before committing to a particular timestep, however, **SmartSpice** will ask Verilog-XL whether there are any digital events occurring (at the interface nodes) within this timestep, and if so, will adjust the timestep to conform. In this way, the two simulators synchronize at all events on the interface nodes, but simulate more or less independently otherwise.
5. When all requested analyses have been performed, both **SmartSpice** and Verilog-XL will terminate.

The SmartSpice Interface to DFII includes a "SmartSpiceVerilog" template for mixed-signal hierarchy configuration; it is essential that the user select this template as the basis for any existing, or new, mixed-signal top-level cells. Once the configuration process has been completed (once, only for each design), the user should be able to successfully partition the circuit under analysis. An

example of a partitioned mixed-signal schematic is shown in figure 1. This is the CCADC example, a 4-bit analog-to-digital converter, which can be found in the Cadence samples directory: the analog, digital and mixed-mode portions of this circuit are color-coded in the normal fashion.

Since **SmartSpice** outputs Cadence Parameter Storage Format (PSF) data files, the results of an analog simulation, or of the analog portion of a mixed-signal simulation, can be plotted in the Cadence Waveform Window, together with any digital waveforms output by Verilog-XL. The analog and digital waveforms resulting from a mixed-mode simulation of the CCADC circuit are shown in figure 2.

In order to make use of **SmartSpice** within the Analog Artist simulation environment, the user will have to purchase from Cadence certain license features. For loading designs into Analog Artist, prior to performing any simulations of any kind and independent of the simulator to be used, the user will first require license feature 34510, the "Artist Design Environment", and to specifically enable access to **SmartSpice** through the OASIS interface, the user will additionally require license feature 32100 (symbolic name: OASIS_Simulation_Interface). Those two features are a necessary and sufficient set for the completion of strictly analog simulations via **SmartSpice**.

In order to perform mixed-signal simulations, independent of the simulator to be used, the user will also require license feature 32140, the "Mixed-Signal Simulation Interface Option", and to actually carry out the digital portion of a mixed-signal simulation the user will require license feature 26000 (symbolic name: VERILOG-XL).