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Intrinsic Capacitance Parameter Extraction in UTMOST III

Introduction

The intrinsic capacitance parameter extraction routine (INTCAP) is in the CAP analysis section of the ***UTMOST III*** MOS module (Routine#67). The INTCAP routine has 5 different intrinsic cap measurements and a "simulation only" capability for all intrinsic caps. Recent developments have improved the INTCAP routine. Users should have ***UTMOST III*** MOS module version 15.2.0 or higher to be able use the examples and explanations presented in this article. The INTCAP routine allows users to measure the MOS capacitances when the device is under DC bias and conducting current.

INTCAP Routine Settings

The intrinsic caps which can be measured using the INTCAP routine are:

CGD, CGS, CGC, CGB and CGG.

The user should select the proper cap using the "Multiple Selection" button located in the "Routine Control" screen for the INTCAP routine. The routine control screen can be opened from the main ***UTMOST*** screen.

The selected cap buttons will appear in red. It is recommended to select one cap at a time for the measurements until the user is familiar with the entire routine.

CGS (Gate to Source Capacitance)

Hardware Connection:

Drain -> DC analyzer (Drain terminal)

Gate -> LCR meter (Low)

Source -> LCR meter (High) AND DC analyzer (Source terminal)

Bulk -> DC analyzer (Bulk terminal)

Operation Principals

The LCR meter will supply the SOURCE Voltage. The DC analyzer SOURCE terminal is also connected to the MOS device SOURCE terminal. However the DC analyzer SOURCE terminal will work as a Voltmeter monitoring the actual SOURCE voltage of the device. The SOURCE voltage needs to be monitored because the LCR meter has an internal shunt resistor at its High terminal and the supplied voltage from the LCR meter and the actual SOURCE voltage are different due to the voltage drop across the LCR meter's shunt resistor. The measured SOURCE Voltage is fed back to ***UTMOST*** and ***UTMOST*** iterates the LCR meter voltage source supply until the device SOURCE terminal reaches to the preset VDS value.

The DRAIN terminal of the MOS device is connected to a voltage supply using the DC analyzer. The DRAIN terminal voltage is stepped to provide the initial VDS voltage before the SOURCE voltage iterations start.

The SOURCE will be stepped to provide the actual VGS voltage steps.

The GATE will be grounded by connecting it to the Low terminal of the LCR meter.

Example:

Conditions: V_{GS}=2V, V_{DS}=1V

Initially the SOURCE voltage (using the LCR meter) is set to -2V to provide VGS=2V. (GATE is grounded)

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The DRAIN voltage (Using the DC analyzer) is set to -1V to provide VDS = -1 - (-2) = 1V.

The MOS device will start conducting some current and there will be a voltage drop at the High terminal of the LCR meter which is connected to the SOURCE. The actual VDS will be different than the preset 1V. The iteration algorithm in ***UTMOST*** will start adjusting the LCR meter voltage supply to provide V_{DS}=1V and V_{GS}=2V.

The monitoring and readjusting of the LCR meter's voltage source is a slow process. During the voltage iterations the actual SOURCE voltage will be displayed on the ***UTMOST*** graphics screen. There is a current limit for each LCR meter. The user should not bias the MOS device to conduct currents which exceeds this limit. During the DC biasing of the device the DC analyzer will be in user mode.

UTMOST Measurement Setup:

V_strt_cgs/d : 0 (vds start voltage)

V_stop_cgs/d : 3 or 5 or 10 (vds stop voltage, can be different based on breakdown).

sweep_points : 15 (# of points used for vds sweep)

VG_start : 0 (vgs start voltage, should be "0" always)

VG_step : 1 (vgs step voltage)

step_points : 4 (# of vgs step)

The remaining "Measurement Variables" are not used for the CGS measurement.

Parameter Extraction

The CGS measurement will produce CGS vs. VDS curves for different step voltages of VGS. The first step curve for VGS = 0V is equivalent of overlap cap measurement curve. The Gate to Source overlap capacitance in BSIM3v3model has 3 components: CGSL + CGSO + CF

CGSL : The overlap cap for the lightly doped region of SOURCE junction.

CGSO : The overlap cap for the heavily doped region of SOURCE junction

CF : The fringing capacitance. If not given it is calculated.

The CGSL is a non-linear overlap capacitance and parameter CKAPPA is used in the overlap cap formula to describe the VGS dependency of CGSL.

The INTCAP routine will extract the CGSO, CGSL and CKAPPA parameters. Press the fit button from the options menu to perform the extraction.

Simulation and Opitimization

The INTCAP routine uses the EXTERNAL SPICE option as a simulator. ***SmartSpice*** is used to simulate the Intrinsic caps.

The CGSO and CGSL can be optimized for the VGS=0V curve. The Initial CKAPPA value can also be optimized using the remaining curves. However since CKAPPA is used for both CGDL and CGSL equations it is better to optimize this parameter using the CGC data (CGC : Gate to channel cap. CGC is the sum of CGD and CGS)

The CLC (Constant term for the short channel Cap model) and CLE (Exponential term for the short channel Cap model) can be optimized using the data other than VGS=0.

CGD (Gate to Drain Capacitance)

Hardware Connection:

Drain -> LCR meter (High) AND DC analyzer (Drain terminal)

Gate -> LCR meter (Low)

Source -> DC analyzer (Source terminal)

Bulk -> DC analyzer (Bulk terminal)

Operation Principles:

The LCR meter will supply the DRAIN Voltage. The DC analyzer DRAIN terminal is also connected to the MOS device DRAIN terminal. However the DC analyzer DRAIN terminal will work as a Voltmeter monitoring the actual DRAIN voltage of the device. The DRAIN voltage needs to be monitored because the LCR meter has an internal shunt resistor at its High terminal and the supplied voltage from the LCR meter and the actual DRAIN voltage are different due to the voltage drop accurs the LCR meter's shunt resistor. The measured DRAIN Voltage is fed back to ***UTMOST*** and ***UTMOST*** iterates the LCR meter's voltage source until the device DRAIN terminal reaches to the preset VDS value.

The SOURCE terminal of the MOS device is connected to a voltage supply using the DC analyzer. The SOURCE terminal voltage is stepped to provide the VGS values.

The SOURCE will be stepped to provide the actual VGS voltage steps.

The GATE will be grounded by connecting it to the LCR meter's Low terminal.

Example:

Conditions: V_{GS}=2V V_{DS}=1V

Initially the SOURCE voltage (using the DC analyzer) is set to -2V to provide V_{GS}=2V. (GATE is grounded)

The DRAIN voltage (Using the LCR meter) is set to -1V to provide V_{DS} = -1 - (-2) = 1V.

The MOS device will start conducting some current and

there will be some voltage drop at the High terminal of the LCR meter which is connected to the DRAIN. The actual V_{DS} will be different than the preset 1V. The iteration algorithm in ***UTMOST*** will start adjusting the LCR meter's voltage supply to provide V_{DS}=1V and V_{GS}=2V.

The monitoring and readjusting the LCR meter's voltage source is a slow slow process. During the voltage iterations the actual SOURCE voltage will be displayed on the ***UTMOST*** graphics screen.

There is a current limit for each LCR meter. The user should not bias the MOS device to conduct currents which exceeds this limit.

During the DC biasing of the device the DC analyzer will be in user mode.

UTMOST Measurement Setup:

V_strt_cgs/d : 0 (vds start voltage)

V_stop_cgs/d : 3 or 5 or 10 (vds stop voltage, can be different based on breakdown).

sweep_points : 15 (# of points used for vds sweep)

VG_start : 0 (vgs start voltage, should be "0" always)

VG_step : 1 (vgs step voltage)

step_points : 4 (# of vgs step)

The remaining "Measurement Variables" are not used for the CGD measurement.

Parameter Extraction

The CGD measurement will produce CGD vs. VDS curves for different step voltages of VGS. The first step curve for VGS = 0V is equivalent of overlap cap measurement curve. The Gate to Drain overlap capacitance in BSIM3v3model has 3 components: CGDL + CGDO + CF

CGDL : The overlap cap for the lightly doped region of DRAIN junction.

CGDO : The overlap cap for the heavily doped region of DRAIN junction

CF : The fringing capacitance. If not given it is calculated.

The CGDL is a non-linear overlap capacitance and parameter CKAPPA is used in the overlap cap formula to describe the VGS dependency of CGDL.

The INTCAP routine will extract the CGDO, CGDL and CKAPPA parameters (Press the fit button from the options menu to perform the extraction).

Simulation and Optimization

The INTCAP routine uses the EXTERNAL SPICE option as a simulator. ***SmartSpice*** is used to simulate the Intrinsic caps.

The CGDO and CGDL can be optimized for the VGS=0V curve the Initial CKAPPA value can also be optimized using the remaining curves. However since CKAPPA is used for both CGDL and CGSL equations it is better to optimize this parameter using the CGC data (CGC : Gate to channel cap. CGC is the sum of CGD and CGS).

The CLC (Constant term for the short channel Cap model) and CLE (Exponential term for the short channel Cap model) can be optimized using the data other than VGS=0.

CGC (Gate to Channel Capacitance)

Hardware Connection

Drain -> Drain and Source are shorted AND connected to LCR meter (Low)

Gate -> LCR meter (High)

Source -> Drain and Source are shorted AND connected to LCR meter (Low)

Bulk -> DC analyzer (Bulk terminal)

Operation Principles:

The LCR meter's high terminal is connected to the GATE of the MOS device. The SOURCE and DRAIN are shorted and connected to the LCR meter's Low terminal. Therefore the DRAIN and SOURCE will always be grounded. The BULK is connected to DC analyzer and its voltage is stepped. The GATE voltage will be swept and CGC will be measured for different VBS voltages. There is no need for Voltage Monitoring for the CGC measurement. Therefore CGC measurement is much faster compared to CGD or CGS measurements.

During the DC biasing of the device (Bulk terminal only) the DC analyzer will be in user mode.

UTMOST Measurement Setup:

VB_start_cgc : 0 (vbs start voltage)

VB_step_cgc : -1 (vbs stop voltage, can be different based on breakdown).

#of_step_cgc : 3 (# of vbs steps)

c_start_bias : -5 (vgs start voltage,LCR meter)

c_stop_bias : 5 (vgs stop voltage, LCR meter)

c_step_bias : 0.1 (vgs step voltage, LCR meter)

The remaining "Measurement Variables" are not used for the CGC measurement.

Parameter Extraction

The CGC measurement will produce CGC vs. VGS curves for different step voltages of VBS. No fitting operation is performed on the CGC data.

Simulation and Optimization

The INTCAP routine uses the EXTERNAL SPICE option as a simulator. ***SmartSpice*** is used to simulate the Intrinsic caps.

The CGDO, CGSO, CGDL, CGSL and CKAPPA can be optimized using the lower cap values portion of the curve. The parameter DLC (channel length reduction on one side for CV model; same as LINT but used for capacitance equations only)can be optimized using the higher cap values portion of the curve.

CGB (Gate to Channel Capacitance)

Hardware Connection:

Drain -> Drain and Source are shorted and connected to DC analyzer(Drain terminal)

Gate -> LCR meter (High)

Source -> Drain and Source are shorted and connected to DC analyzer(Drain terminal)

Bulk -> LCR meter (Low)

Operation Principles:

The LCR meter's High terminal is connected to the GATE of the MOS device.

The BULK is connected to the LCR meter's Low terminal (grounded).

The DRAIN and SOURCE are shorted and connected to the drain terminal of the DC analyzer.The drain terminal voltage will be stepped. This means both VD and VS voltages are stepped together.

The GATE voltage will be swept and CGB will be measured for different VD & VS voltages. There is no need for Voltage Monitoring for the CGB measurement. Therefore CGB measurement is much faster compared to CGD or CGS measurements.

During the DC biasing of the device (Drain terminal only) the DC analyzer will be in user mode.

UTMOST Measurement Setup:

VD_start_cgb : 0 (vd & vs start voltage)

VD_step_cgb : 1 (vd & vs stop voltage, can be different based on breakdown).

#of_step_cgb : 3 (# of vd & vs steps)

c_start_bias : -5 (vgb start voltage,LCR meter)

c_stop_bias : 5 (vgb stop voltage, LCR meter)

c_step_bias : 0.1 (vgb step voltage, LCR meter)

The remaining "Measurement Variables" are not used for the CGB measurement.

Parameter Extraction

The CGB measurement will produce CGB vs. VGB curves for different step voltages of VD & VS. No fitting operation is performed on the CGB data.

Simulation and Optimization

The INTCAP routine uses the EXTERNAL SPICE option as a simulator. ***SmartSpice*** is used to simulate the Intrinsic caps. This data is used to verify previously extracted parameters.

CGG (Total Gate Capacitance)

Hardware Connection:

Drain -> Drain, Source, Bulk are shorted and connected to LCR meter (Low)

Gate -> LCR meter (High)

Source -> Drain, Source, Bulk are shorted and connected to LCR meter (Low)

Bulk -> Drain, Source, Bulk are shorted and connected to LCR meter (Low)

The DC analyzer is not used for CGG measurement

Operation Principles:

The LCR meter's High terminal is connected to the GATE of the MOS device.

The DRAIN, SOURCE and BULK are shorted and connected to the LCR meter's Low terminal (grounded).

The GATE voltage will be swept and CGG will be measured. This is a single curve measurement. There is no additional voltage stepping and there is no need for the DC analyzer connection. CGG is a typical total Gate Capacitance measurement and it is accomplished using only the LCR meter.

UTMOST Measurement Setup:

c_start_bias : -5 (vgg start voltage,LCR meter)

c_stop_bias : 5 (vgg stop voltage, LCR meter)

c_step_bias : 0.1 (vgg step voltage, LCR meter)

The remaining "Measurement Variables" are not used for the CGG measurement.

Parameter Extraction

The CGG measurement will produce a CGG vs. VGS curve. The CGG data is used to extract the Oxide Thickness (TOX). Select the Fit option from the Options menu to execute the parameter extraction.

Simulation and Optimization

The INTCAP routine uses the EXTERNAL SPICE option as a simulator. ***SmartSpice*** is used to simulate the Intrinsic caps.