

# Simulation Standard

Connecting TCAD To Tapeout

A Journal for Process and Device Engineers

## Validation of *CLEVER* Interconnect Parasitics with 0.18 $\mu\text{m}$ Process Measurements

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### Motivation

*CLEVER* can perform accurate field solver extractions of resistance and capacitance from 3D structures generated from realistic process simulation. Comparison of *CLEVER* results with measurements made by SGS-Thomson Microelectronics were done to validate the simulator. Validation was done for a state-of-the-art process applicable to 0.18  $\mu\text{m}$  technology. The process has the following features:

- multiple dielectrics
- conformal deposition around conductors
- inter-metal fill with low-k dielectric
- non rectangular metal cross sections

### Process Description

The aim of the validation exercise is to make comparison of simulated and measured capacitances. To achieve this it is necessary to be very precise in the description of the process steps. The capacitances for deep sub-micron structures are

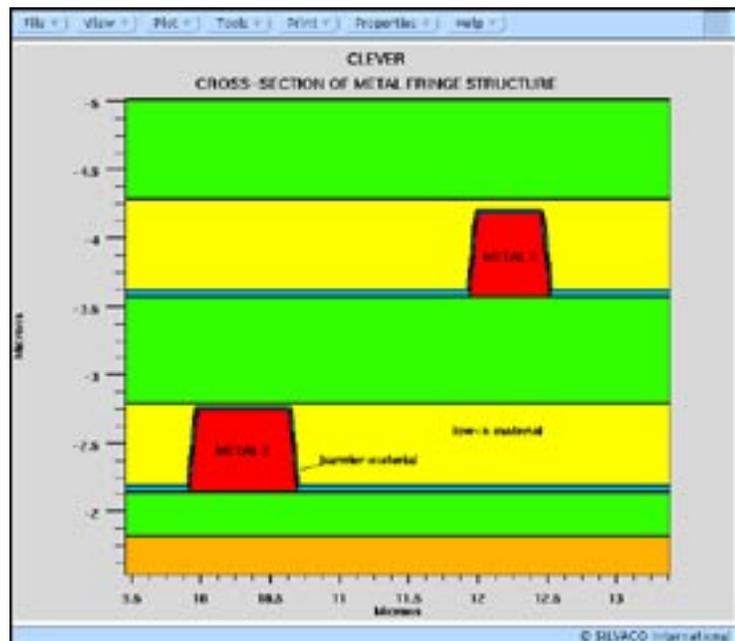


Figure 2. *CLEVER* simulation of low-k process matched to SEM in Figure 1.

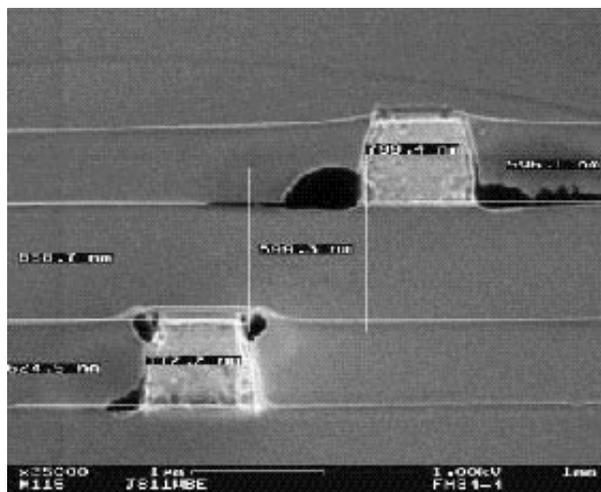


Figure 1. SEM of interconnect cross-section for a low-k process.

highly dependent on process geometry especially for multi-dielectric technologies. *CLEVER* was used since it is designed to model interconnect parasitics by simulating the 3D back end process in a very accurate manner due to its advanced process models for photolithography deposition and etching [1].

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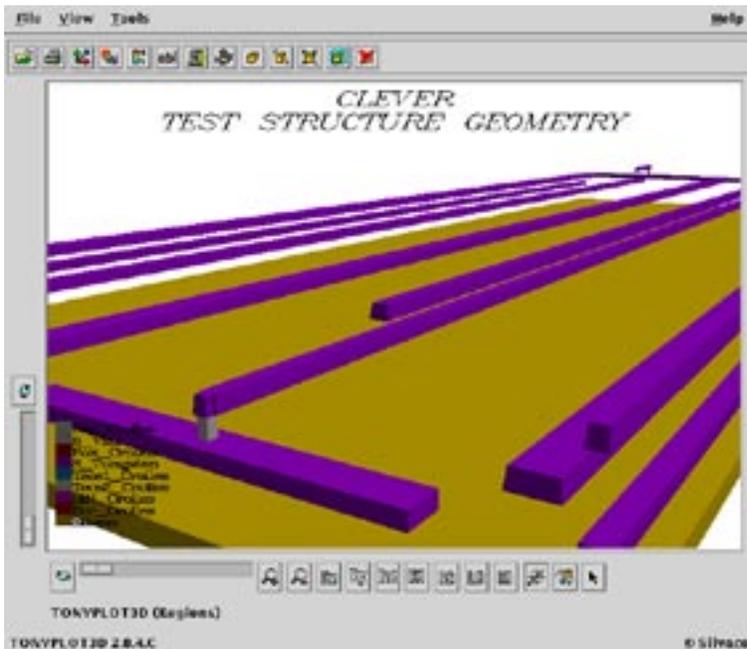


Figure 3. Process simulation resulting in a Non-Manhattan geometry of the metal 3 layer.

The measurements and *CLEVER* simulations were carried out with the ST HCMOS7X process. The pitch is 1um and the part of SiO<sub>2</sub> usually deposited by plasma (ECR), is replaced by a low-k material gapfill (Fox). The Fox thickness target is around 600nm. The permittivity of Fox deposited between metal line is around 3, whereas the dielectric constant of the TEOS capping layer is 4.2. However, there is a slight variation on these values due to the process dispersion. It is assumed that these fluctuations are under 5% of the initial value.

The process architecture for the metals 2, 3 and 4 is the same. The metal stack thickness (Ti + Al + TiN) target is 610nm. A TEOS liner of 50nm is deposited on the stack. In the two following steps, Fox and TEOS are deposited. After CMP, the capping layer thickness that remains on the Fox is around 900nm.

### CLEVER Simulations

To be confident in reproducing the real process SEM photographs were used to optimize the process simulation steps. Based on these SEM observations it was possible to judge whether the simulation can be done using the faster Manhattan mode or more accurate Non-Manhattan mode (Figure 3). The tradeoff being to increase the speed of simulation.

In addition the SEMs were able to show if during the process underetching or overetching occurred which can lead

to a modification of width and space between materials. Adjustments can be made for this in *CLEVER* or through modifying the layout (Figure 4).

Using a consistent methodology the simulation of 14 patterns was performed (Figure 4). In order to have the ability to vary some parameters during the simulation a parametrized input file was used (Figure 5). By using variable parameters in the input file it is possible to see the impact of the variation of the permittivity of the low-k dielectric, for example, on the capacitance in a simple way. To verify if the simulation result is quite similar to the real process the Ruler feature in *TonyPlot* was used to check thickness, space etc. (Figure 2).

## Measurement Method Principle

### ARPIC Method

Full details of the measurement system can be found in [2]. Different patterns coming from a technology independent environment called ARPIC are measured. ARPIC generator and circuit are described in the context of a 1606 interconnect patterns circuit implemented in a 6-metal layer, standard CMOS process with the use of a sub-femto-farad charged-based capacitance measurement (CBCM) driver. This matrix that contains the 1606 cells consists of 73 rows and 22 columns. Each cell includes two different capacitive loads and a driver.

One box contains the capacitances of the physical environment in which targeted capacitance will be measured

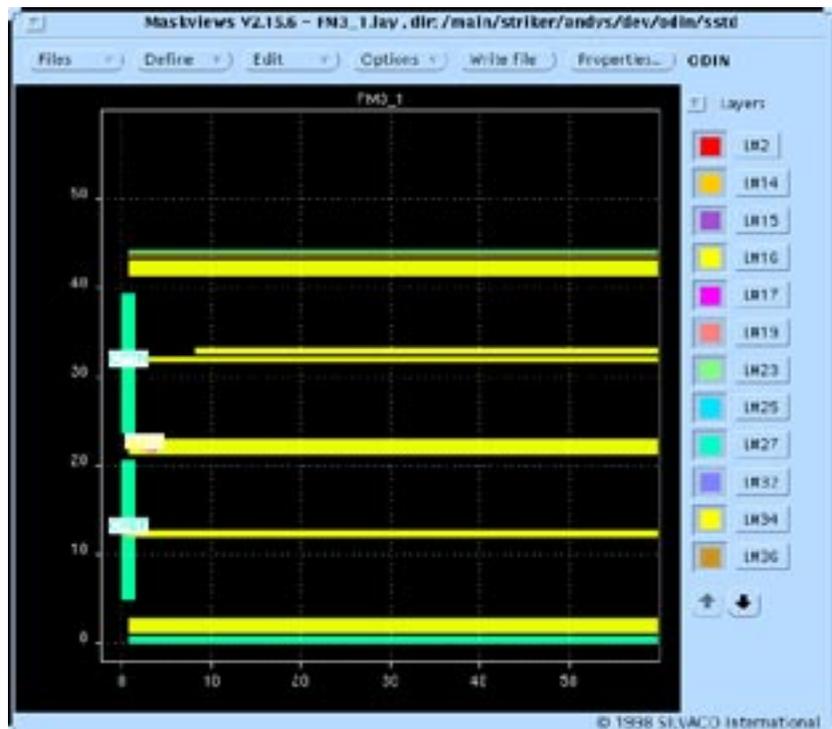


Figure 4. An example of a layout used for simulation. Note the dimension of 100um \* 50um.



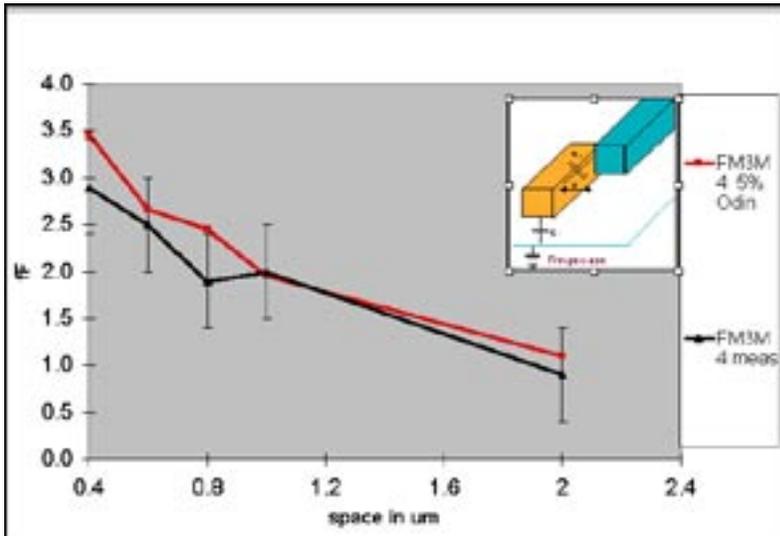


Figure 7. Comparison between simulation ( $\square$ ) and measurements ( $\Delta$ ) or different layer fringe or edge capacitance. Two parallel lines of  $0.6\mu\text{m}$  width and  $100\mu\text{m}$  length with one line in metal 3 and the other of metal 4.

## Experimental Description

The comparison between simulation and measurements is done on 14 different quasi-2D patterns. Results are shown 6, 7 and 8. The physical slice of 3D-patterns composed for example of two crossing lines, is very difficult : two perpendicular slices have to be done on the same pattern to note the elementary dimensions (oxide and metal thickness, metal width, etc.).

The 14 patterns can be divided into three groups:

A: FM3 (Fringe Metal 3) : two parallel lines of a  $0.6\mu\text{m}$  length in metal 3, are separated by 5 different spaces. The results are shown in Figure 6.

This configuration permits analysis of the cross talk phenomena. Another interest is to see the advantage brought by the low-k dielectric material, Pox, substituted for  $\text{SiO}_2$ , on the intra-metal-capacitance.

B: FM3M4 (Fringe Metal 3 Metal 4) : two parallel lines of a  $0.6\mu\text{m}$  width and a  $100\mu\text{m}$  length with one line made of metal 3 and the other one of metal 4. The space between line has also 5 different values :  $s = 0.4\mu$ . This configuration could put forward how edge effects are taken into account by *CLEVER*. Results are in Figure 7.

C: PM3M4 (Plane Metal 3 Metal 4) : one plate of metal 3 is below a plate of metal 4 with no overhang (the 2 plates have the same width and are parallel). The length is  $100\mu\text{m}$  again. W takes 4 different values :  $0.6\mu\text{m}$ ,  $0.8\mu\text{m}$ ,  $1.4\mu\text{m}$ ,  $5\mu\text{m}$ . Results are in Figure 8.

## Validation Summary

Figures 6, 7 and 8 show the comparison of measured and simulated results for the three patterns described above. All results show good matches. Most are well within the limitations of the measurement resolution.

*CLEVER* has been demonstrated to model accurate interconnect parasitics for a state-of-the-art metal process featuring conformally deposited barrier materials around non-rectangular metal lines and low-k dielectric fillers.

For LPE rule like generation using the same accuracy, *EXACT* can be used since it is using the common 3D process simulation techniques.

## References.

- [1] Simulating Accurate 3D Geometries for Interconnect Parasitic Extraction using *CLEVER*. Simulation Standard August 98
- [2] B. Borot "ARPIC: Automatic Representation Of Patterns For Interconnect Characterization"
- [3] J. Chen. "An on-chip, interconnect capacitance characterization method with sub-femto-farad resolution", ICMS March 97.

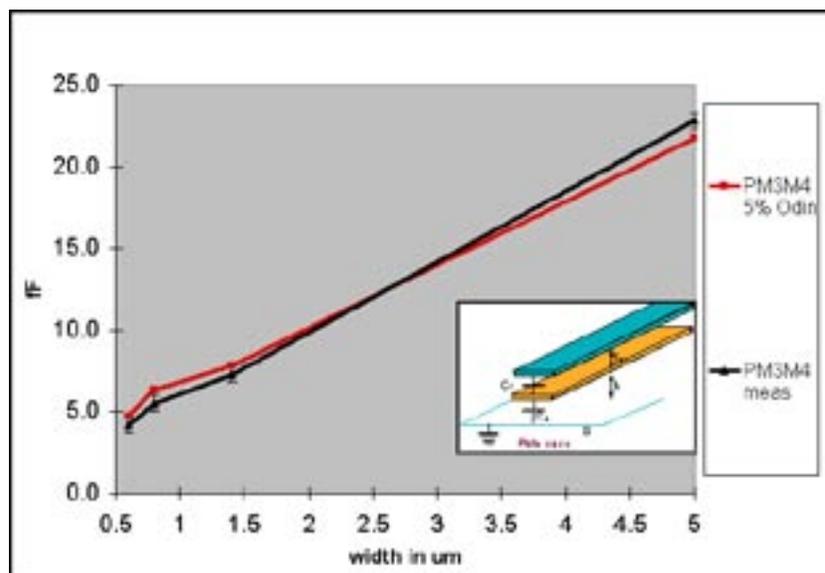


Figure 8. Comparison between simulation ( $\Delta$ ) and measurements ( $\square$ ) for two stacked lines. Two parallel lines of metal 3 and metal 4 without any overhang.

# Accurate, High Speed Physics in *FastBlaze*

## Ultra-Fast Simulation Technique

*FastBlaze* uses novel device simulation techniques to simulate typical MESFET and HEMT characteristics in less than a minute. To be a truly useful engineering tool this extremely high speed must be achieved without compromising the accuracy of the physical models. In practice the speed of *FastBlaze* allows the use of more advanced models than are usually considered for conventional device simulation.

Four areas of modeling in *FastBlaze* are highlighted here to demonstrate the necessity of using the most accurate available device physics when simulating MESFETs and HEMTs.

## Impact Ionization Models

In conjunction with the DC and RF analysis, *FastBlaze* also simulates breakdown by including impact ionization models. The Selberrherr and the second and third order Crowell-Sze, Toyabe and Concannon models are supported with tuned coefficients for GaAs. *FastBlaze* includes an automated DC IV point algorithm which samples IV points only in regions where the current is changing. This algorithm has been enhanced to handle the sharp turning points produced as breakdown occurs. Figure 1 shows breakdown occurring in a double-recessed GaAs MESFET.

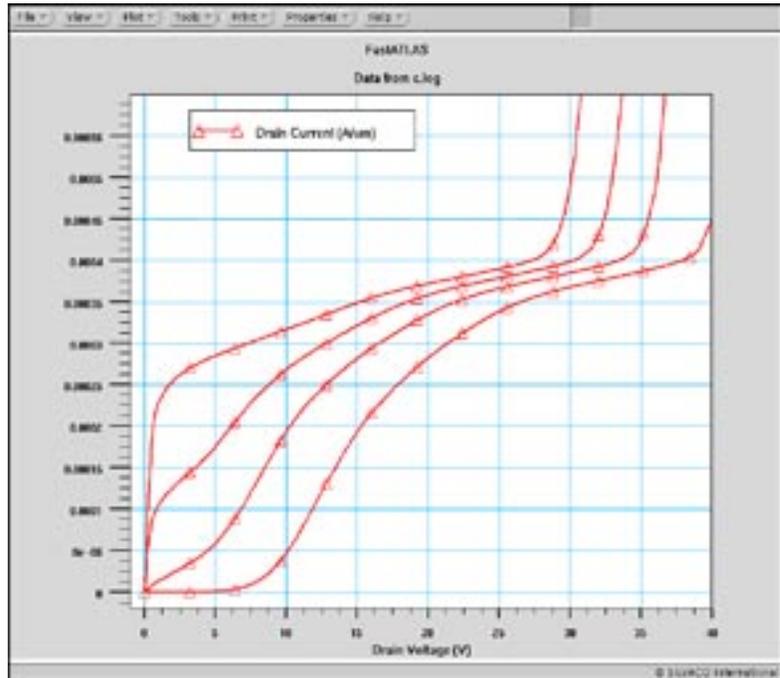


Figure 1. Breakdown occurring in a double-recessed GaAs MESFET

## Ionized Traps

*FastBlaze* includes state-of-the-art charge models, namely the inclusion of quantum mechanics via the self-consistent solution of Schrodinger's equation. Further, incomplete impurity ionization is included for both dopants and traps allowing accurate simulation of DX centers and surface pinning. Figure 2 illustrates the carrier profile across an InGaAs/InP heterojunction generated by the quantum simulation.

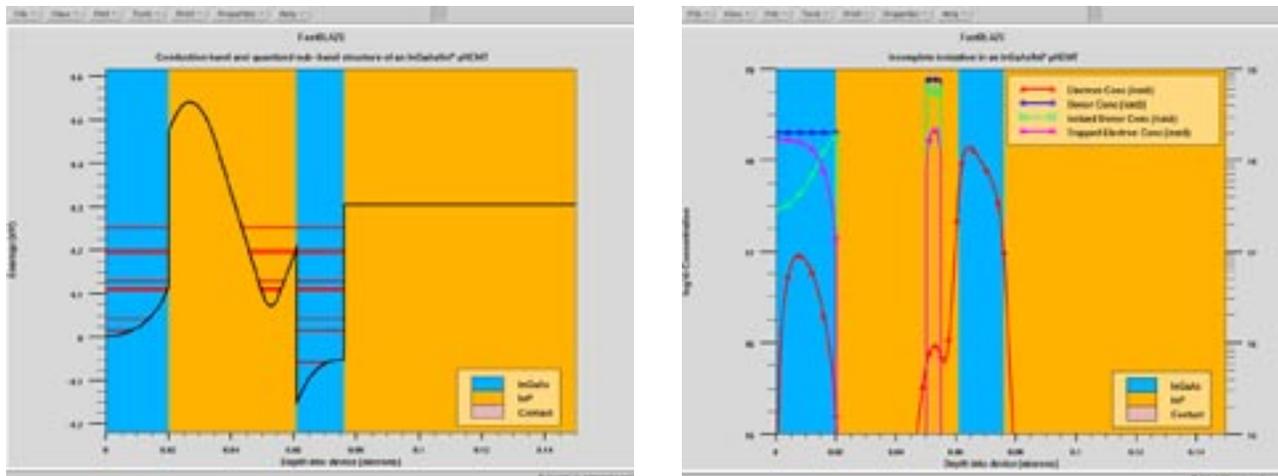


Figure 2. Comparison of complete and incomplete donor ionization. As the conduction band edge dips below the Fermi-level the shallow donor sites trap electrons, reducing the net doping level.

## Multi-Layer Model Specification

*FastBlaze* implements a sophisticated multi-layer transport technique that includes a wide selection of default models. The conventional analytic field dependent models are supplemented by a comprehensive Monte-Carlo derived transport database providing users with unequaled resources important for accurate simulation. In addition core device models can be replaced with user-defined code using the C-Interpreter allowing device engineers unparalleled freedom.

*FastBlaze* permits different mobility, energy-field and impact-ionization models to be declared in different epitaxial layers. Figure 3 illustrates the effect of limiting a device simulation to one transport model. Here the DC-IV family of curves are compared for an AlGaAs/GaAs pseudomorphic HEMT simulated using a simple one-model approach and the more accurate multi-layer models. Note in the multi-layer simulation the material transport parameters are extracted from the Monte Carlo transport database.

## C-Interpreter

*FastBlaze* incorporates an updated version of the C-language Interpreter used by other Silvaco products. This allows users to add their own models for:

- mobility as a function of doping, field and lattice temperature.
- impact ionization
- relation of hydrodynamic energy (carrier temperature) to electric field equivalent to energy relaxation time
- DC gate conduction
- doping distribution
- incomplete ionization

The new C-Interpreter incorporates a graphical debugger and a set of debugging syntax for efficient prototyping of models. The interpreter pre-processes the user supplied code resulting in only a small decrease in overall simulation time compared with the built-in models.

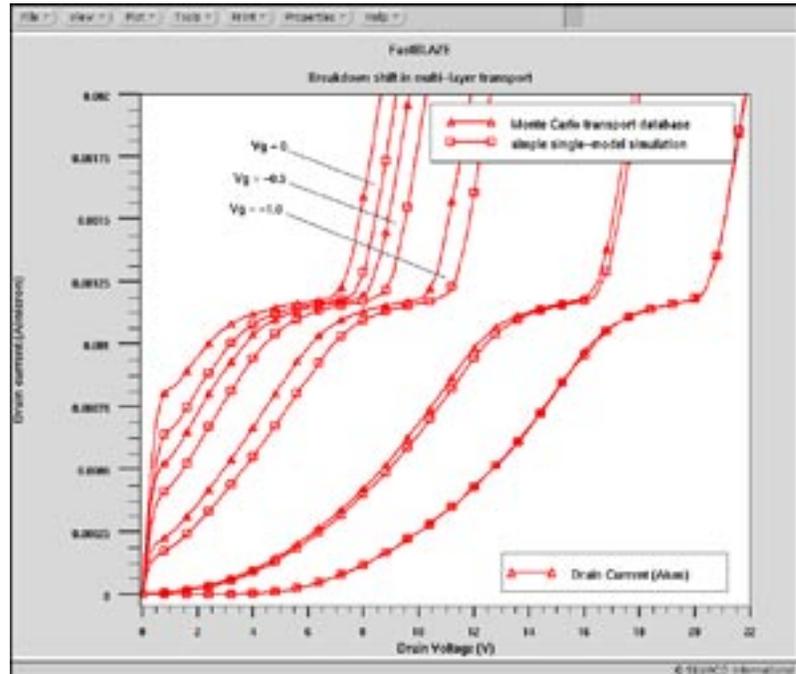


Figure 3. *FastBlaze* incorporates multi-layer transport models. Here an AlGaAs/InGaAs/GaAs pseudomorphic HEMT is simulated using the Monte-Carlo derived transport models and compared with the simple one-mobility model results. The effect on breakdown is illustrated.

## Conclusion

The four models described above demonstrate the standard of models required for accurate device simulation of III-V FET devices; note *FastBlaze* only simulates devices using the full hydrodynamic energy - balance models. *FastBlaze* incorporates these features and is able to model most DC characteristics inside 30 seconds and RF characteristics inside 2 minutes. This combination of speed and accuracy makes *FastBlaze* an ideal tool for interactive TCAD.

Model	Simulation Options
mobility:	Monte Carlo Database standard "Silicon type" analytic velocity overshoot analytic C-interpreter
hydrodynamic energy-field relationship (equivalent to energy relaxation time):	Monte Carlo Database standard field-dependent analytic C-interpreter
DC gate leakage current:	none (perfect insulator) thermionic emission C-interpreter
impact ionization:	Selberrherr Crowell-Sze (2 <sup>nd</sup> and 3 <sup>rd</sup> order) Toyabe Concannon C-interpreter

Table 1. Summary of physical models in *FastBlaze*.

# Calibrating a Typical Bipolar Process Flow

## Introduction

A common request from TCAD (Technology Computer Aided Design) users is advise on how to calibrate the process flow and device simulator to a particular technology. In this article, guidelines are presented for calibration of process and device simulations for a typical poly-emitter bipolar process. Such a process would be used to create a structure shown in Figure 1. Unlike a MOSFET process where calibration mostly takes place in the process simulation, calibration of a bipolar process will include parameters in both the process and device simulators. A simple procedure is presented here that highlights the most important parameters that require calibration and indicates the expected region of the gummel plot over which each variable has the most influence.

## Calibration Method

The reader is presumed to be familiar with the basic operation of *ATHENA* and using appropriate models for each process step. For example, the incorrect use of diffusion models defined in the "method" statement, for example, will invalidate the rest of this following section.

Calibrating a bipolar process flow initially entails matching the two parameters, base current and collector current, to measured results throughout the full operating range of the device. By implication the current gain of the device ( $I_c/I_b$ ) will also be matched. All of the following paragraphs refer to the standard plot of collector and base currents measured against the base-emitter voltage,  $V_{be}$ , unless it is specifically stated otherwise. This standard I-V graph is usually referred to as the "Gummel Plot".

Another way of plotting the same information in a different format is a plot of current gain,  $h_{fe}$ , versus the log of the collector current. This graph, however, is less clear as to which current is increasing or decreasing for each change of current gain. This graph is less useful for understanding variation of the collector and base currents.

The full operating range of a bipolar junction transistor (BJT) consists of three general regions defined by the current density injected into the base. These three operating regions are usually described as the low, medium and high current injection regimes. The medium injection

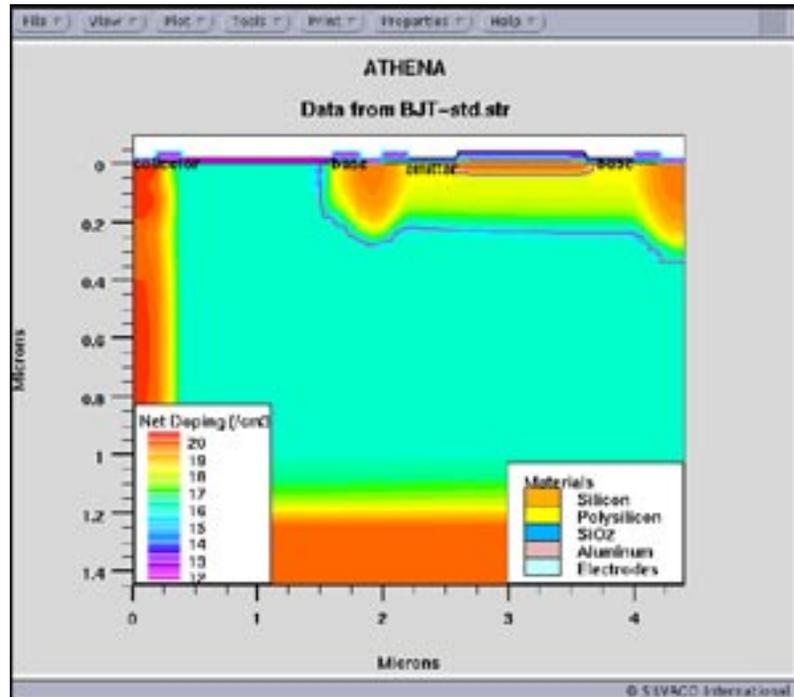


Figure 1. NPN bipolar transistor geometry and doping from *ATHENA*.

region is the most important part of the curve to model correctly as this represents the typical operating condition of the BJT. Each of the three operating regions is dominated by a different physical phenomenon. Successful modeling of a BJT involves matching both the base and collector currents in each of the three general operating regions making a total of six areas for calibration. The derived parameter,  $h_{fe}$ , is also a good parameter to monitor, since this is sensitive to errors in the ratio of collector to base current.

## Identifying Five Calibration Targets

The following text suggests an approach and describes which of the five regions are affected by each change. The general technique is to calibrate the parameters that have the greatest effect on device performance in all regions first and then move to more subtle phenomenon that affect certain parts of the base or collector currents. In general, matching the collector current for all injection regions is less problematic than matching the base current at the extremes of the injection regions and so there are more sections on tailoring these parts of the curve. The text is therefore divided up into the following sections:

- (i) Tuning Base and Collector Currents - All Regions

- (ii) Tuning the Base Current -  
All Regions
- (iii) Tuning the Collector Current -  
All Regions
- (iv) The Base Current Profile -  
Medium Injection
- (v) The Base Current Profile -  
Low Injection

If the above order is followed, there should be a reasonable correlation between measured and simulated data. However, most of the tuning parameters have some degree of inter-dependency, the degree of which is also device design specific, so some degree of iteration of the tuning parameters is to be expected.

When tuning bipolar transistors, there is a greater emphasis in tuning device parameters, compared to optimizing MOSFETs where most tuning parameters are process related. A powerful combination is the tuning of a BiCMOS process where the MOSFET part of the process flow can be used to tune the process parameters while the bipolar part of the flow is used to tune the device simulator. This technique should yield a high degree of predictability in the results.

Tuning the process simulation parameters in *ATHENA* is mainly required to model effects such as the implantation induced defect enhanced diffusion, responsible for the "emitter push effect" which is essential to obtain the correct depth of the base-collector junction. The correct process modeling of the out diffusion of dopant from the poly-emitter into the mono-crystalline substrate is also critical to obtaining well matched I-V curves. Another critical process modeling area is the base implant as it is essential to match measured and modeled base resistance for correct modeling of the collector current. These and other issues are discussed in the sections below.

### **(i) Tuning Base and Collector Currents - All Regions**

One important parameter to model the general level of base and collector currents is the device measurement temperature. The base and collector currents are strongly influenced by temperature changes as small as a few degrees centigrade. A significant effort should be made to determine the exact temperature of the device during measurements before calibration is attempted and this temperature should be input into the device simulator, *ATLAS*, in the `MODELS` statement using the `TEMPERATURE=<>` parameter. An increase in temperature will cause an increase in base and collector currents.

### **(ii) Tuning the Base Current - All Regions**

A critical region for poly-emitter bipolar devices is the interface between the poly emitter and the mono-crystalline silicon. This region is difficult to process simulate directly as the interface between the poly-silicon emitter and single crystalline silicon usually consists of a thin, uneven and possibly non continuous film of oxide. The way this is simulated is by calibrating the overall affect of this interface, not with a process simulator but with the device simulator, *ATLAS*. The tuning parameter is the surface recombination velocity at this interface for electrons (`VSURFN` for PNP devices), or holes (`VSURFP` for NPN devices).

The surface recombination velocity parameter only affects the base current but affects the base current in all operating regions. It is therefore a powerful parameter to approximately match the base current and gain throughout the full operating range. In some cases the base current may be less affected in the very high and very low injection regions by changes in the surface recombination velocity adding some scope to fine tune the profile of the base current versus base-emitter voltage curve.

It is important to realize that the poly emitter **MUST** be defined as an electrode in order to be able to define the interfacial surface recombination velocity, `VSURFN` and `VSURFP`, using the `CONTACT` statement. This is in contrast to the MOSFET calibration text where it is strongly advised not to define the poly-gate as an electrode. Be sure not to get these two confused. The parameter that activates the recombination velocity is `SURF.REC` also in the contact statement. For an NPN BJT for example:

```
CONTACT NAME=emitter N.POLYSILICON SURF.REC \
VSURFP=1.5e5
```

A lower value of recombination velocity, `VSURFP` will reduce the base current and increase the gain, `hfe`. The converse is also true.

### **(iii) Tuning the Collector Current - All Regions**

The parameter which affects the collector current over the entire range is the intrinsic base resistance. The base resistance is primarily determined by the dose of the base implant(s). An increase in the base implant dose will decrease the intrinsic base resistance and decrease the collector current in all injection regions. In some cases, however, the collector current may be only slightly affected in the very high injection region giving scope for fine tuning the profile of collector current versus base-emitter voltage.

If the pinched or intrinsic base sheet resistance is a measured parameter, the simplest way to match measured and simulated data is to make slight changes to the base implant dose within the expected error actual implanted dose in conjunction with the error in percentage activation.

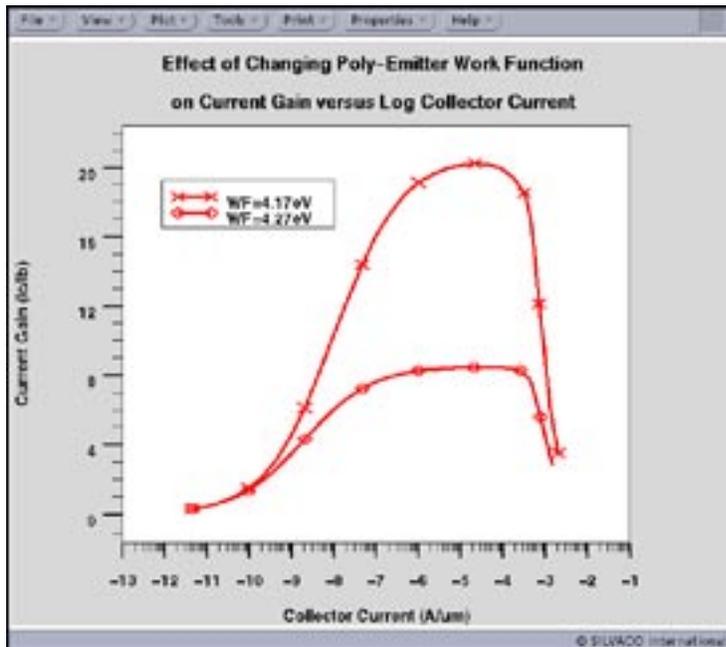


Figure 2. Effect of emitter contact workfunction on bipolar gain.

In some designs, where the base contact is close to the collector contact or the base contact is large, such as the substrate contact, the collector current may also be influenced in all current injection regions by specifying a surface recombination velocity at the base contact. For a typical design with a buried n+ collector and surface contacts, the surface recombination velocity at the base contact may have little effect on the collector current

#### (iv) The Base Current Profile - Medium Injection

There are two major parameters in *ATLAS* that have a significant effect on the base current in the medium injection regime, these being the workfunction of the poly-emitter and the band-gap narrowing affect. These two affects are described in sections (a) and (b) below.

##### (a) Poly-emitter work function

If the poly-emitter is described as `N.POLYSILICON` in the `CONTACT` statement for an NPN device as described in section (iii) above, the work function of the poly-emitter is set to 4.17V and is correct for saturation doped n++poly-silicon. If, however, the poly-emitter is not saturation doped, the work-function will differ from this ideal and have a pronounced affect on the base current and current gain in the medium injection regime. The work function of the poly-gate can vary from 4.17V for n++ poly-silicon to  $(4.17V + E_g)$  for p++ poly-silicon depending on the position of the Fermi-Energy. Changing the work-function of the poly-emitter by just 0.1V from 4.17V to 4.27V can often halve the current gain in the medium injection regime as shown in the current gain plot of Figure 2. It is therefore very important to assign

the correct value. The contact statement below assigns a workfunction of 4.27eV to the poly-emitter, whilst keeping the other parameters the same as before:

```
CONTACT NAME=emitter SURF.REC
VSURFP=1.5e5 \
WORKFUN=4.27
```

The poly-emitter workfunction can be calculated by measuring the position of the fermi-energy at the poly-silicon/silicon interface relative to the conduction band and adding this value to 4.17V. For example, if the Fermi-energy is measured as being 0.1eV from the conduction band edge, the workfunction of the poly-emitter set in the contact statement should be set to  $4.17 + 0.1 = 4.27V$ .

##### (b) Band-gap Narrowing Effects

If the `BIPOLAR` parameter is stipulated in the `MODELS` statement in *ATLAS*, bandgap narrowing is included automatically. The inclusion of bandgap narrowing in the `MODELS` statement is strongly advised since this phenomenon has a significant effect on the current gain of the device. However, in order to validate the default Klaassen bandgap narrowing model, the Klaassen mobility model should also be used. This is activated by using the additional keyword `KLA` to the models statement. For example:

```
MODELS BIPOLAR KLA
```

will correctly activate the Klaassen bandgap narrowing model. The parameters in the Klaassen band gap narrowing model are user definable in the `MATERIAL` statement. There are three user definable parameters for the Klaassen band gap narrowing model. The `BGN.E` parameter has a linear dependency on doping concentration and has the default value of  $6.92e-3$  volts. `BGN.C` has a square root dependency with doping concentration and has the default value of 0.5. `BGN.N` is the value of doping where band gap narrowing effectively starts to take affect and has a default value of  $1.3e17/cm^3$ . The equivalent default setting would therefore be written as:

```
MATERIAL BGN.E=6.92e-3 BGN.C=0.5 \
BGN.N=1.3e17
```

These parameters can therefore be altered to modify the current gain of the device in the medium injection regime. For example, reducing the linear parameter from  $6.93e-3$  to  $6.5e-3$  is sufficient to cause a significant reduction in current gain in the medium injection region. The band gap narrowing parameters affect both collector and base currents but affect the base current to a greater magnitude. The most sensitive plot to see the effects of small changes to the band gap narrowing is a plot of current gain versus log of collector current. A reduction in band gap narrowing will result in an increase in current gain in the medium current injection region.

## (v) The Base Current Profile - Low Injection

This is one case where there is an interdependency on one parameter, since the intrinsic base resistance not only affects the collector current in all regions (see above) but it also has an effect on the base current in the low injection region as shown in the gummel plot of Figure 3.

For a small range of implant doses around the optimum, the base doping concentration will also affect the position of the knee and/or the rate of falloff of the base current in the low injection operating region of the device. This is most noticeable as a loss of current gain in the low injection region for the alternative standard plot of current gain versus collector current. An increase in the base implant reduces the intrinsic resistance and typically decreases the base current in the low injection region resulting in an increase in current gain for very low currents.

A similar affect to increasing the base doping is observed if the base doping is kept constant but the overall doping is reduced in the mono-crystalline silicon region of the emitter. The doping profile in the mono-crystalline region of the emitter can be tuned using three parameters in the process simulator.

The main physical affect of these *ATHENA* parameters is to change the doping profile of the emitter in the mono-crystalline silicon. These three parameters are:

- 1/ the grain structure in the poly-emitter.
- 2/ the dopant segregation effects in the poly-emitter.
- 3/ the dopant velocity across the silicon/poly-silicon boundary.

The first parameters will affect how quickly the dopant in an implanted poly-emitter reaches the silicon/poly-silicon boundary during the RTA diffusion and therefore affects the total diffusion of dopant into the single crystalline part of the emitter and hence the base width doping profile. The *POLY.DIFF* diffusion model is used.

The second parameter affects dopant pile-up at the poly-silicon/silicon boundary and hence the source doping concentration at the monocrystalline interface. Once again, therefore, this will affect the overall doping profile of the emitter in the mono-crystalline region of the device.

The third parameter affects the velocity of transport of dopant across the poly-silicon/silicon boundary with similar affects to the parameters above.

These parameters can be used to tailor the emitter doping profile in the mono-crystalline silicon region to match available measured data,

usually in the form of SIMS or capacitance information. An accurate profile of dopant in the poly-silicon part of the emitter is not too important if measured data concerning interfacial dopant concentrations is available. This is because the work function of the poly-emitter is going to be set in *ATLAS*, the device simulator, by defining the poly-emitter as an electrode. All that is required to calculate the correct work function at the poly-silicon emitter is the interfacial doping concentration at the poly-silicon/silicon interface on the poly side of the junction. Setting the correct workfunction for the poly-emitter is described in section (iv-a) above.

## Conclusions

Following the methodology presented here and by using a logical combination of tuning parameters available to the user in *ATHENA* and *ATLAS*, a good match for bipolar transistors should be obtainable for most device designs.

Since it is usually less problematic to match the collector current for all levels of applied base-emitter voltage compared to the matching of base current, the user will probably find that more time is spent trying to match the base current for very small and very large values of applied base-emitter voltage. The user should ensure, however, that great attention is placed on making sure that the correct process models are used in the process flow to reduce the overall uncertainty as to which parameters require calibration.

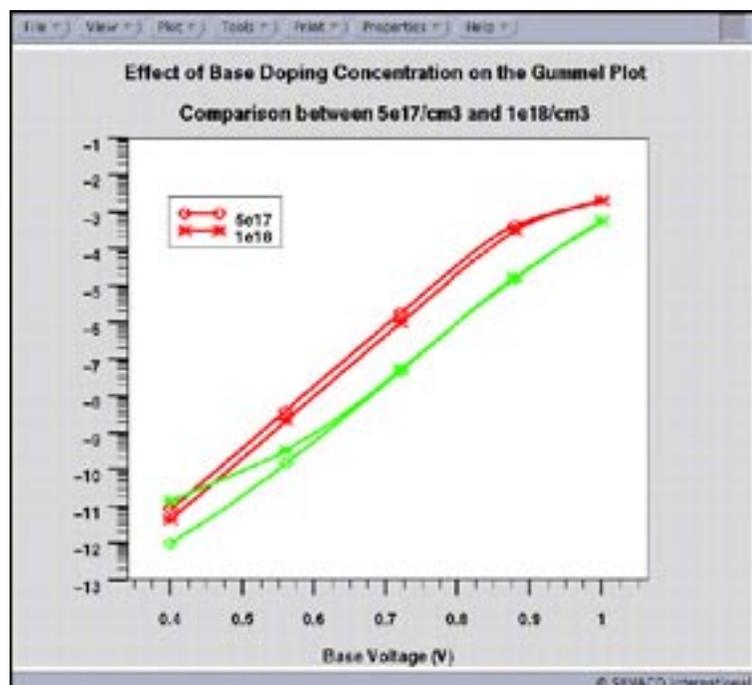


Figure 3. Effect of base doping profile on low injection base current in BJT.

# New Model for High Energy Implants in *ATHENA*

## Introduction

In our earlier paper [1] a new Binary Collision Approximation (BCA) module was described. It was shown that models and algorithms implemented into the BCA module allow to accurately predict implant profiles with significant channeling as well as the dose and screen oxide thickness dependencies for relatively low implant energies.

Recently, this module was extended into 2D and completely integrated with *ATHENA*. Implementation of the BCA module will allow *ATHENA* users simulate 2D implant profiles with accuracy which could not be achieved even with the best experimentally verified analytical models (e.g. SVDP). The main advantage of the BCA approach is its ability to simulate profiles for those conditions for which reliable experimental results do not exist. Also, experimental 2D profiling techniques are still unique, very expensive, and yet to become widely available. Therefore, there are no experimentally verified tables of lateral moments which could be used for 2D analytical simulations.

This paper is focused on simulation of medium and high energy implants. Since upper energy limits for SVDP model are 100 keV for Boron and 180 keV for Phosphorus and Arsenic, it is reasonable to consider medium energies starting from upper SVDP limits up to ~1 MeV and high energies above 1 MeV. These implant energies are widely used in different technologies. Double and triple well formation in CMOS technology using multiple medium and high energy implants is a very important application.

## BCA Model Description

In the BCA, the deflection of the trajectories of moving particles is calculated in a strictly binary way - between the moving atom and the closest atom in the lattice. The ion implantation is simulated by following the fate of

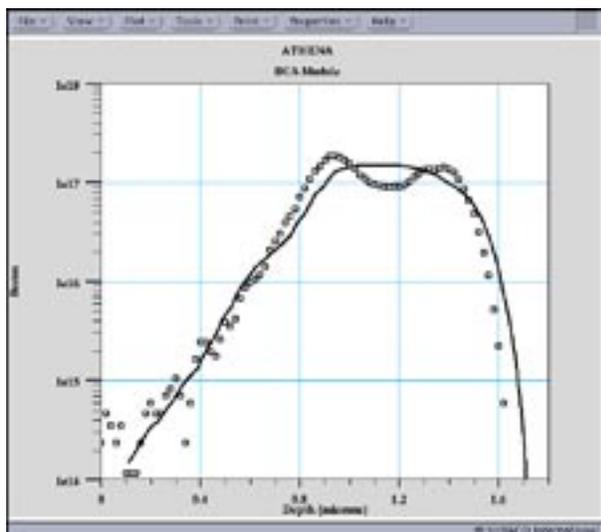


Figure 2. Comparison of BCA simulation ( $\square$ ) and measurement for a 380keV Boron implant at zero degrees. The simulation is within the resolution of the measurement technique.

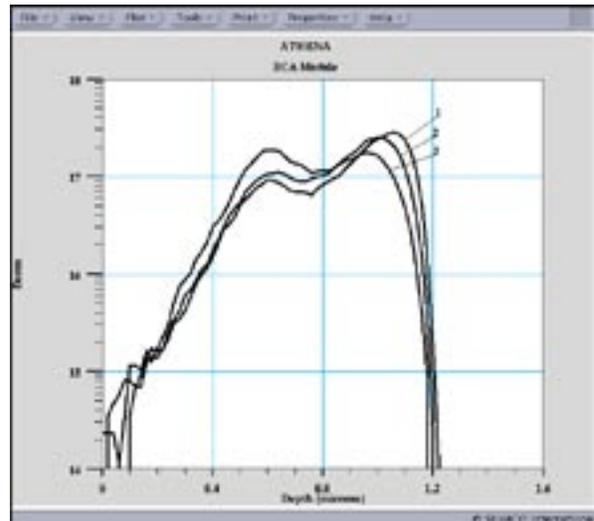


Figure 1. Effect of beamwidth on zero tilt 200 keV low dose boron implant.

- 1: beamwidth = 0;
- 2: beamwidth = 0.5 degrees;
- 3: beamwidth = 1.0 degree.

a large number of sequentially generated pseudo-projectiles, each of which carries an equivalent dose corresponding to a fluence increment obtained by dividing the total fluence by the number of pseudo-projectiles and scaled for the topography under interest.

The atomic collisions are considered to be composed of a quasi elastic part and of an essentially separate electron excitation part. The barycentric scattering angle is evaluated with the MAGIC formula [2]. The program uses the screened Coulomb potential with the universal screening function described in [2]. The screening length in the calculation is the universal one proposed in [2]. In order to properly account for the channeling, the BCA module uses non local and local inelastic energy loss models. The local impact dependent inelastic energy loss model is the exponential model suggested by Oen and Robinson [3]. The damage accumulation is based on the displacement model of Kinchin and Pease [4].

## Simulation Results and Comparison with Experiments

### Boron

Zero tilt angle, medium energy boron implant simulation is the most challenging problem. From one side, the experimental profiles are very sensitive to even slight changes in the experimental setup including precise surface orientation and ion beam direction and beam width. From the other side, simulation results are very sensitive to details of local electronic stopping models. Figure 1 shows the effect of beamwidth on low dose zero

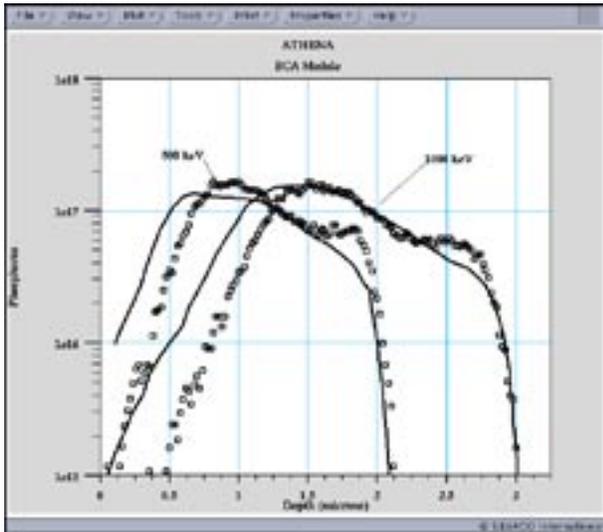


Figure 3. Zero degree phosphorus implants simulated using the BCA model ( □ ) compared to measured data.

tilt, 200 keV boron implant into  $\langle 100 \rangle$  direction. The BCA simulation profiles demonstrate two distinctive peaks: random scatter and channeling. The height ratio between the peaks strongly depends on ion beam width or divergence. In the ideal case of absolutely collimated beam the crystalline peak is  $\sim 3$  times higher than the amorphous peak. In the case of beamwidth = 1 degree (incident ion directions are uniformly distributed between  $-1$  and  $1$  degree) the scatter peak becomes higher. The experimental profiles do not always show these distinctive peaks but rather have a wide plateau as in Figure 2. The difference could be attributed both to possible uncertainties in experimental setup and to inaccuracy of local electronic stopping model. Currently implemented generic local electronic stopping model does not take into account details of the electron distribution in the  $\langle 100 \rangle$  channel.

Figure 2 shows that the above analysis is valid for a higher energy of 380keV.

## Phosphorus

Figure 3 compares simulated and experimental [6] profiles for 500 keV and 1000 keV,  $1.5 \times 10^{13}$  ions/cm<sup>2</sup> Phosphorus implants at zero degree tilt along  $\langle 100 \rangle$  axis. As expected the second peak is much lower than for comparable boron energies. In these cases agreement is even better than for boron implants because local electronic stopping for channeling phosphorus is less dependent on peculiarities of electron distributions.

## Arsenic

Figure 4 shows simulated and experimental [7] 300 keV As profiles. They do not have the second peak but rather characteristic long tails.

## Conclusion

It is shown that the BCA module recently integrated into *ATHENA* under the *MC Implant* module could be used for quite accurate simulation of medium and high energy (up to 1 MeV) implants in  $\langle 100 \rangle$  direction of crystalline Silicon. In separate simulations the validity of implemented stopping power models is confirmed for off axis boron implants with energies up to 3 MeV. Simulated results are close to experimental data when limits of the experimental accuracy are considered. Our BCA implementation is 5 to 10 times faster than UT-MARLOWE [8] which allows practical use for high energy implant simulations. The BCA module can be used for extraction of spatial moments for our computationally efficient 2D model described in [9].

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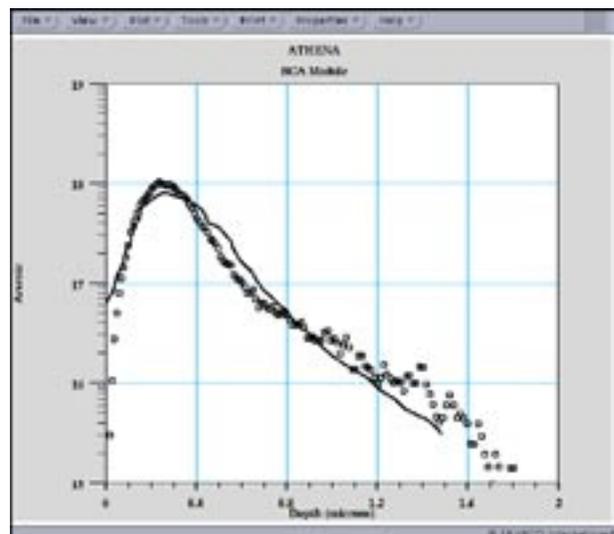


Figure 4. 700 keV Arsenic implant simulated by the BLA model ( □ ) and compared to measured curve.

# Calendar of Events

## November

1	GaAs IC - Atlanta, CA
2	GaAs IC - Atlanta, CA
3	GaAs IC - Atlanta, CA
4	GaAs IC - Atlanta, CA
5	
6	
7	
8	ICCAD - San Jose, CA
9	ICCAD - San Jose, CA
10	ICCAD - San Jose, CA
11	ICCAD - San Jose, CA
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18	W/S Tokyo - Celebrity
19	W/S Tokyo - Discovery
20	W/S Tokyo - UTMOST III
21	
22	
23	
24	
25	
26	Happy Thanksgiving
27	
28	
29	
30	

## December

1	
2	
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7	IEDM - San Francisco
8	IEDM - San Francisco
9	IEDM - San Francisco
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18	
19	
20	
21	
22	
23	
24	
25	Merry Christmas
26	
27	
28	
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31	

## Bulletin Board



### FastBlaze Shines at GaAs '98

Silvaco's new *FastBlaze* will steal the show at the GaAs IC Symposium in Atlanta. From November 1st through 4th, attendee focus will be on the power of the extremely fast quasi-2D simulator. Providing accurate characteristics for DC transients, AC up to arbitrary high frequencies, and spontaneous distributions such as potential, electric field, and band diagrams.



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Visit suite 957 at ICCAD November 9th through the 11th for the cutting edge of industry technology. Use our breakthrough hierarchical editor and design rule checker tools, *Expert* and *Savage*. Check your designs for density, performance, and reliability by checking out what Silvaco can do for you!



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See what the future holds for you in TCAD and Parasitic Interconnect Simulation, as the San Francisco Hilton and Towers will host both IEDM '98 and Silvaco International on December 7th through the 9th. At the Powell Room on the sixth floor, a large staff of Silvaco application engineers will demonstrate the latest in TCAD simulation, parasitic interconnect extraction and circuit simulation.

For more information on any of our workshops, please check our web site at <http://www.silvaco.com>

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# Hints, Tips and Solutions

Andy Strachan, Applications and Support Manager

**Q: How can anti-reflective coatings be modeled when simulating photodetectors in ATLAS/Luminous? How can detection efficiency be plotted?**

Earlier version of ATLAS were able to handle refraction and reflection of rays during the optical simulation in Luminous. New features have been added to ATLAS version 4.4.25 or higher to include coherence and so allow simulation of the effects of anti-reflective coating.

The simulation of photodetector efficiency versus wavelength is done using the LAMBDA parameter of the SOLVE statement. This parameter sets the wavelength for each solution. A new ray trace is done at each solution point to recalculate the optical intensities. The syntax might be:

```
SOLVE B1=1 LAMBDA=0.6 INDEX.CHECK
```

The parameter B1 sets the intensity of the light source #1 in Watts/cm<sup>2</sup>. A useful parameter INDEX.CHECK is recommended for use here. It reports the real and imaginary parts of the refractive indices of each material involved in the ray trace calculation. This can be useful to check the default parameters for refractive index especially at very high or low wavelengths.

The INTERFACE statement is used to define the properties of the anti-reflective layer on the top of the silicon. Note that the layer does not need to be physically present in the structure defined for ATLAS.

```
INTERFACE AR.INDEX=2.05 AR.THICK=0.05
```

The parameters AR.THICK defines the ARC thickness in microns. Most commonly this is a quarter wavelength of the light taking into account the wavelength in the ARC material. AR.INDEX defines the real part of refractive index of the ARC. This is ideally the square root of the substrate material refractive index.

Figure 1 compares the spectral response of the cases with two thickness of ARC and without the ARC. Note the increase around 550nm wavelength for the 70nm ARC. The detection efficiency is defined as the ratio of

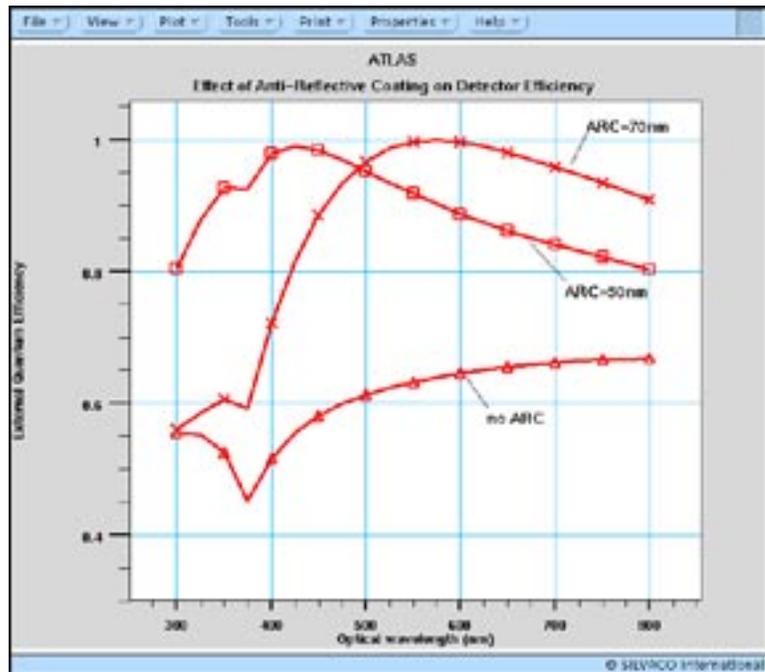


Figure 1. Comparison of detector efficiency for different anti-reflective coating thickness.

two parameters. This quantity can be plotted using the functions in *TonyPlot*.

*source photocurrent* is the amount of current generated by the light source. *available photocurrent* is the amount of current absorbed by the semiconductor. Differences between these two are due to reflection, transmission or absorption in non-semiconductor materials. The ratio of available photocurrent/ source photocurrent is often known as *external quantum efficiency*. An alternative approach using the ratio of actual terminal current from the detector to the source photocurrent is also possible.

In this example the ARC is planar and non-absorbing. The light is also normally incident. ATLAS also has features to model the ARC with non-normal incidence. More complex cases such as absorbing ARCs can be modeled by using user-defined equations in the C-Interpreter function for reflection, F.REFLECT.

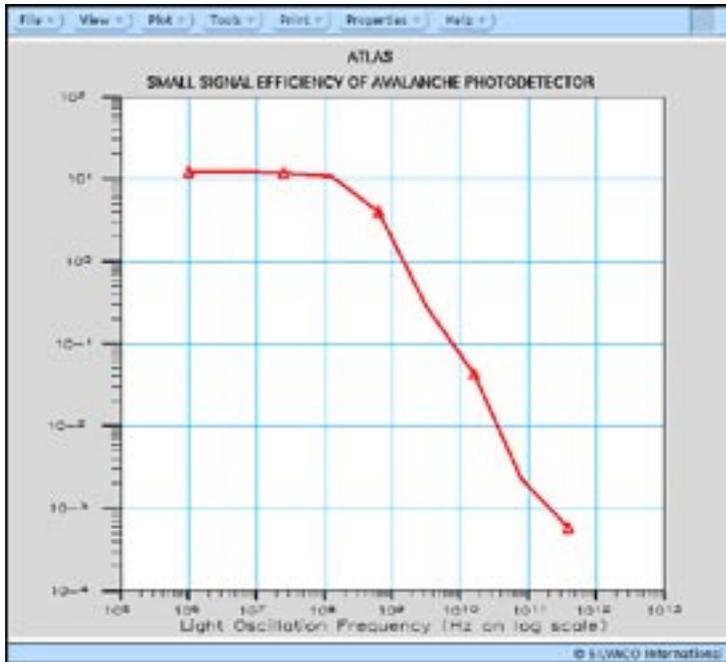


Figure 2. Response of avalanche photodetector with respect to frequency of light oscillator.

**Q: Can a similar detection efficiency be plotted against an oscillation frequency of the light?**

Small signal analysis for light beams is available in *Luminous* in a similar manner to the AC voltage analysis for electrical simulations.

The syntax to do this is:

```
SOLVE B1=1 SS.PHOTO FREQ=1E6 FSTEP=5 MULT.F
\ NFSTEPS=8 BEAM=1
```

The parameter `SS.PHOTO` enables the small signal light oscillations. The frequency parameters operate as in electrical simulations to control the initial frequency, frequency step size and number of steps to ramp the frequency. The `BEAM` parameter specifies the light beam to be ramped.

Figure 2 shows the results of small signal light response for an avalanche photodetector. The y-axis is detector efficiency defined as terminal current divided by the source photocurrent. Since the detector has carrier multiplication through impact ionization the efficiency at low frequencies is greater than unity.

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