Simulation Standard

Connecting TCAD To Tapeout

A Journal for Process and Device Engineers

Ultra-Fast Device Simulation with Monte Carlo Tuned Transport Models in *FastBlaze*

FastBlaze is a fast physical device simulator for MESFETs and HEMTs optimized to provide interactive TCAD for modern III-V FET devices. It incorporates device-specific techniques to allow 1000x to 10000x simulation speeds compared to conventional device simulation. ***FastBlaze*** is the first simulator in the ***FastATLAS*** framework and covers III-V material models for isothermal DC and RF simulation of FETs.

Sophisticated Physical Models

FastBlaze does not compromise in the accuracy of the physical models in order to obtain fast simulations. In practice the speed of ***FastBlaze*** allows use of the most complex and advanced models without the huge speed penalty seen in conventional device simulation. Highlights of the physical models in ***FastBlaze*** are:

- ***Monte Carlo Generated Material Parameters***
  The Monte Carlo simulator ***Mocasim*** was used to derive carrier velocity characteristics for common III-V materials. Models are derived as a function of field, doping, mole fraction and temperature. Figure 1 shows the electron velocity as a function of doping and field for GaAs. Figure 2 shows the function for different materials.

- ***Energy Balance Simulation***
  FastBlaze uses energy balance simulation by default. The energy and momentum relaxation times as a function of carrier energy, doping, mole fraction and temperature are also obtained from **Mocasim.** These provide the most accurate representation of velocity overshoot and non-local transport possible.

- ***Quantum Mechanics***
  FastBlaze provides quantum statistics for describing carrier distributions in quantized channel regions. A Schrodinger solver is used to calculate and plot the quantized energy levels at any bias. Figure 3 shows the conduction band of a InGaAs HEMT with the first eleven bound-state energy levels.

- ***Multi-Layer Transport***
  FastBlaze uses a true multi-layer transport scheme where material parameters are layer dependent. This is important for HEMTs and also for devices with complex impurity and trap distributions. (See Figure 4)

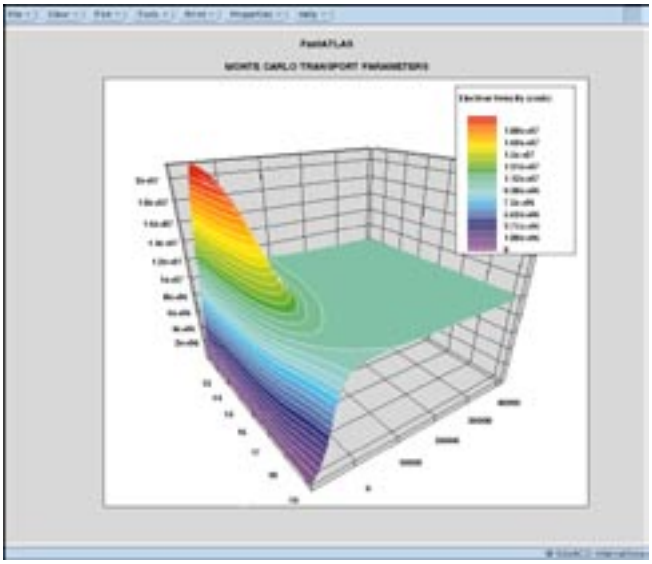

Figure 1. Monte Carlo generated electron velocity as a function of doping and field. This data is used by FastBlaze for accurate carrier transport simulation.

- ***Bulk and Interface Traps***
  Typically the trap densities in III-V FETs can greatly affect the device performance. **FastBlaze** allows definition of multiple trap states both for bulk traps such as EL2 and interface surface states. Figure 5 shows the trap distribution in a typical FET structure in **FastBlaze .**

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INSIDE

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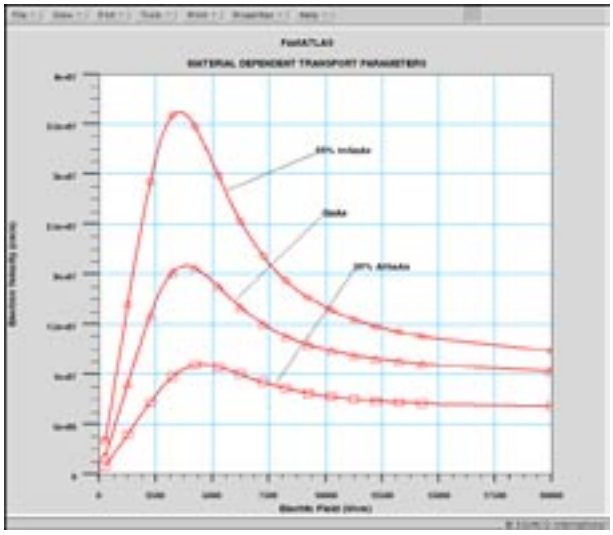

Figure 2. Velocity-field characteristics for various III-V materials.

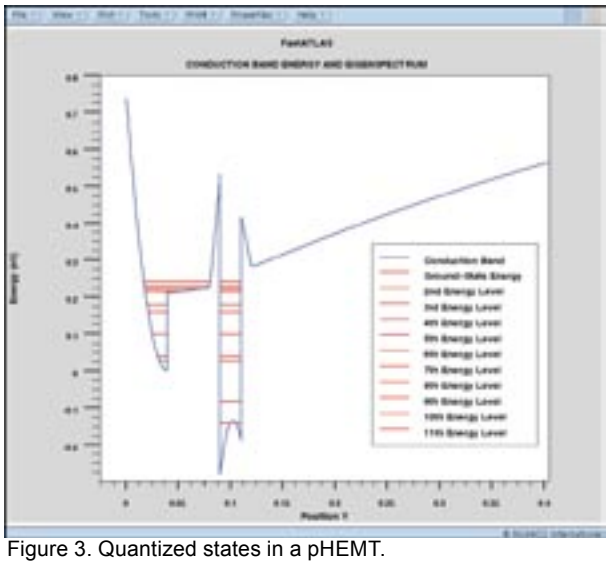

Figure 3. Quantized states in a pHEMT.

Interactive TCAD

FastBlaze was written entirely in-house at Silvaco to meet commercial development standards. For the average user it is important to marry the sophisticated physics with a simulator that is easy to use and is well supported. Important features that move towards interactive use of TCAD have been included in the development. Seamless integration is done with the ***VWF*** framework and the interactive tools ***DeckBuild*** and ***TonyPlot.*** In addition the following key features make ***FastBlaze*** easy to use for non-TCAD experts:

- ***FastATLAS specific GUI***
  A dedicated GUI as part of ***DeckBuild*** allows rapid prototyping of FET structures including epitaxy and doping definition. The interface supports the definition of complex multi-recess structures with multiple impurity and trap doping profiles. Figure 6 shows the GUI used to define a pHEMT.

- ***Interactive Graphics***
  FastBlaze interfaces both I-V data and 2D electrical distributions of physical parameters to ***TonyPlot.*** Full 2D plots of potential, field and current density can be obtained. ***TonyPlot*** supports both polar plots and Smith charts for analyzing RF parameter data.

- ***Automated, adaptive meshing***
  The user does not need to do any mesh definition or refinement when using ***FastBlaze.*** The automatic mesh algorithm applies a very high mesh density to critical areas of the FET structure. Although the typical simulation time in ***FastBlaze*** is less than 1 minute the number of mesh points is around 7000 node points.

- ***Parameter Variations and Experimentation***
  With such fast simulation speeds the ability to run many device structure variations becomes very attractive for device development or characterization. Figure 7 shows an experiment with various recess depths.

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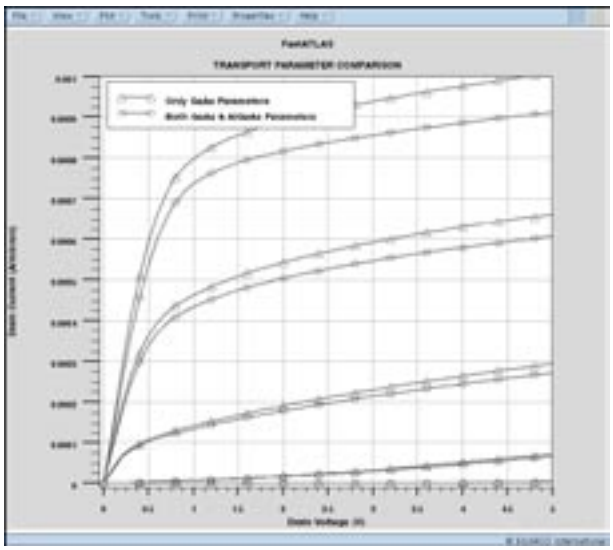

Figure 4. Comparison of HEMT Id-Vd using correct multi-layer transport models. The AlGaAs transport parameters are derived from Mocasim.

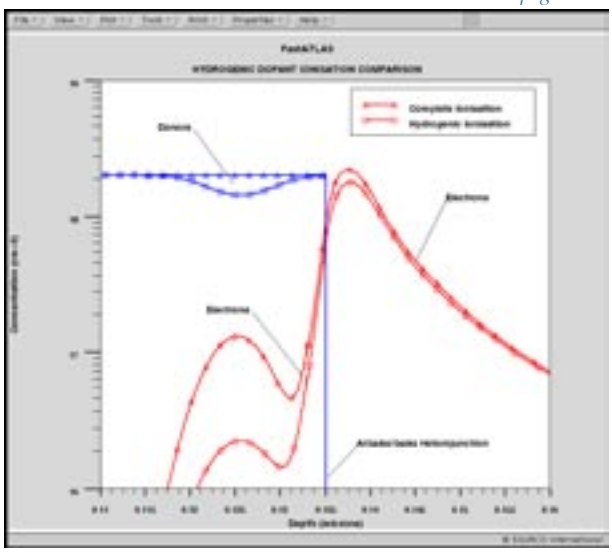

Figure 5. Effect of incomplete ionization on dopant and carrier densities. Both traps and dopant impurities have several occupation statistic models.

ATLAS/MixedMode Simulation of a Three Stage CMOS Ring Oscillator

Part I: MixedMode Setup

Introduction

Ring oscillator circuits are a valuable test structure for determining the feasibility and success of an integrated circuit process fabrication sequence. One of the most useful results obtainable from a ring oscillator test structure is the delay time per gate. This information is especially important for successful design of high speed clock circuits, such as Phase Locked Loops (PLL's) and Voltage Controlled Oscillators (VCO's).

This article is aimed at demonstrating the simulation of a three stage CMOS ring oscillator. Using ***ATLAS/MixedMode***, MOSFET devices in the circuit are simulated numerically. For Part I, both NMOS and PMOS devices were created with analytical doping profiles using ***ATLAS***. In Part II these devices will be created from process simulation using ***ATHENA*** and process variations will be analyzed. *Part II will be published in the next issue of the Simulation Standard.*

MixedMode simulation provides the capability to simultaneously solve the device and circuit equations using fully coupled algorithms. This allows circuit simulation including devices for which no compact SPICE model exists. In addition, device creation in ***ATHENA*** can yield the optimum process conditions for a given device or the effects of process variations on circuit performance.

Mixed Circuit/Device Simulation

The schematic diagram of a three stage CMOS ring oscillator is shown in Figure 1. Each NMOS device in the circuit is defined in ***ATLAS*** using the `REGION`, `ELECTRODE`, and `DOPING` statements (Figure 2), resulting in the structure shown in Figure 3. PMOS devices are defined in a similar manner, but with opposite doping polarity. These virtual devices along with the load capacitors (C1=C2=3fF and C3=6fF) are used to define the ring oscillator circuit in ***MixedMode***. The syntax used is included in Figure 6, where the device name, node designation, corresponding structure file, and width are specified for each device.

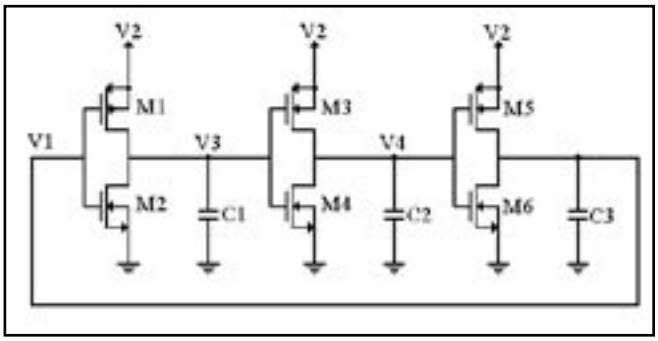

Figure 1. Schematic Diagram of Three Stage CMOS Ring Oscillator Used in MixedMode Simulation.

```
#    Regions
region      num=1 y.min=0 silicon
region      num=2 y.max=0 oxide

#    Electrodes
elec        num=1 x.min=1 length=1.0 name=gate
elec        num=2 left    length=1.0 y.min=0 y.max=0 name=source
elec        num=3 right   length=1.0 y.min=0 y.max=0 name=drain
elec        num=4 substrate name=substrate

#    Doping profiles
doping uniform conc=1e16 p.type
doping gauss   conc=1e17 p.type char=0.2  peak=0.15
doping gauss   conc=1e20 n.type junc=0.17 x.right=1.0 ratio=0.7
doping gauss   conc=1e20 n.type junc=0.17 x.left=2.0  ratio=0.7
```

Figure 2. ***ATLAS*** Statements Used to Define the NMOS Device for MixedMode Simulation.

Simulation commences by applying a piecewise linear waveform (0 to 5 volts) with a rise time of 50 picoseconds to the supply voltage (V2 in Figure 1). Transient analysis of the circuit is carried out for 800 picoseconds, providing a few periods of oscillation. The voltages versus time at nodes one, three, and four are plotted in Figure 4. The onset of oscillation is readily seen between zero and approximately 300 picoseconds, where the peak to peak magnitude of V[1], V[3], and V[4] increases until reaching a maximum after 300 picoseconds.

From the time variation of voltage at node one, the delay time for each gate can be determined from the following equation [1,2]

$$\tau = \frac{T}{2n} \quad (1)$$

where T is the period of oscillation, and n is the number of gates in the ring oscillator circuit. From Figure 4, the period is estimated to be approximately 315 picoseconds, and thus the delay per gate using Equation 1 is determined to be approximately 52.5 picoseconds.

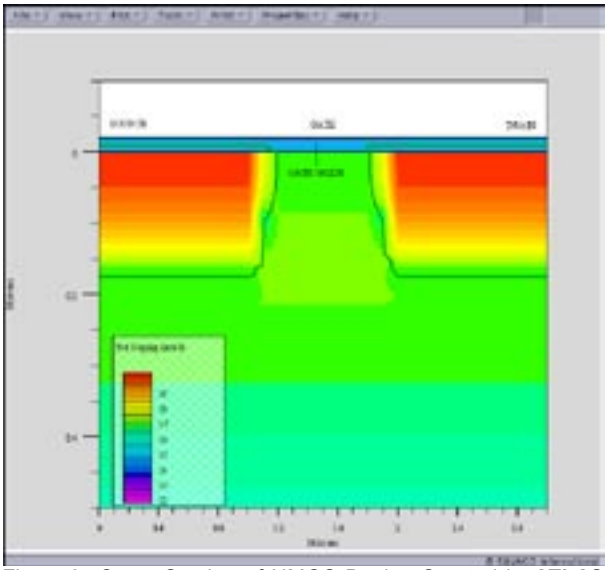

Figure 3. Cross Section of NMOS Device Created in ***ATLAS*** and Used in ***MixedMode*** Simulation.

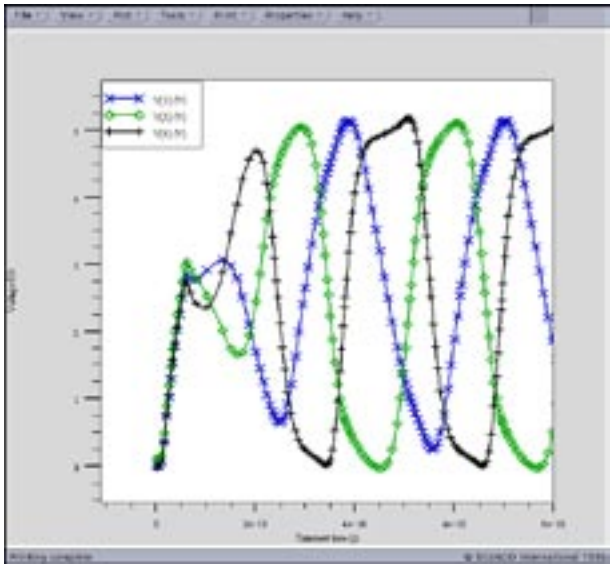

Figure 4. Three Stage CMOS Ring Oscillator Node Voltages Versus Time.

Switching operation of one inverter stage is shown in Figure 5, where drain currents are displayed in the top half, and node voltages V[3] and V[4] are displayed in the bottom half. When V[3] is at a maximum or minimum value, the corresponding drain currents are very small. As V[3] transitions from the maximum or minimum values, the drain currents begin to increase toward their maximums.

Summary

The simulation of a three stage ring oscillator in ***ATLAS/ MixedMode*** has been demonstrated. Definition of the individual MOSFET devices was accomplished using analytical doping profiles in ***ATLAS***. Examining process variations using ***ATHENA*** will be investigated in Part II. *Part II will be published in the next issue of the Simulation Standard.* Example syntax of device definition and specification in the ring oscillator circuit was included. The gate delay was extracted from the transient analysis output voltage versus time.

References

[1] T. Ohzone, T. Miyakawa, T. Matsuda, T. Yabu, and S. Odanaka, "Performance Evaluation of CMOS Ring-Oscillators with Source/ Drain Regions Fabricated by Asymmetric/Symmetric Ion-Implantation," Proc. IEEE 1997 International Conference on Microelectronic Test Structures, Monterey, California, pp. 131-136, March 1997.

[2]. A. Mahajan, G. Cueva, M. Arafa, P. Fay, and I. Adesida, "Fabrication and Characterization of an InAlAs/InGaAs/InP Ring Oscillator Using Integrated Enhancement and Depletion Mode High-Electron Mobility Transistors, " IEEE Electron Device Letters, Volume 18, Number 8, pp 391-393, 1998.

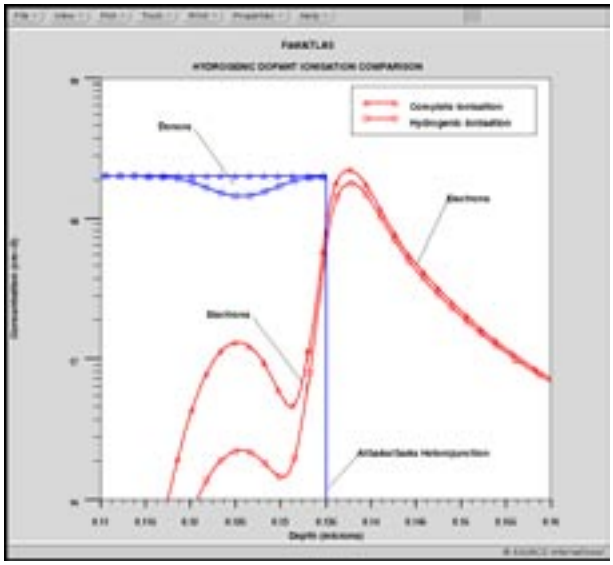

Figure 5. Switching Operation of One CMOS Inverter Stage. Drain Currents (top) and Node Voltages (bottom).

```
aM1 3=drain 1=gate 0=source 0=substrate infile=nmos.str width=5.
aM2 3=drain 1=gate 2=source 2=substrate infile=pmos.str width=15.
c1 3 0 3ff
vdd 2 0 0
aM3 4=drain 3=gate 0=source 0=substrate infile=nmos.str width=5.
aM4 4=drain 3=gate 2=source 2=substrate infile=pmos.str width=15.
c2 4 0 3ff
aM5 1=drain 4=gate 0=source 0=substrate infile=nmos.str width=5.
aM6 1=drain 4=gate 2=source 2=substrate infile=pmos.str width=15.
```

Figure 6: Statements Used in ***MixedMode*** Simulation to Define Three Stage CMOS Ring Oscillator Circuit

Low-Power Systems-on-a-Chip CAD

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Introduction

Mixed-signal systems-on-a-chip (SOC) integration of digital, analog, RF, and power components is emerging to meet demands for low-power, highly integrated systems in portable computing, wireless communications, and multimedia. Applications are also found in transportation [1] and in aerospace/defense. Lithography scaling trends are fueling this development, with RF performance now possible from bulk CMOS. Deep submicron devices, however, are increasingly sensitive to second-order effects with the result that traditional circuit simulations cannot accurately predict performance without first accounting for specific device structures and layout topography. The complex interaction between digital switching logic and analog or RF continuous wave circuits further complicates simulation and modeling. Described below are the tools necessary for SOC design and modeling, as well as two applications examples based on research being conducted at the Systems on Silicon Research Center (SYSREC) at the University of Illinois at Chicago (UIC).

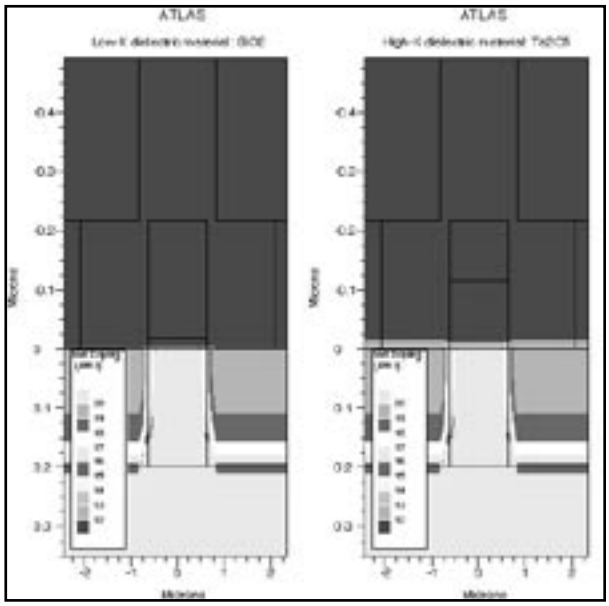

Figure 1. Device structures constructed in DEVEDIT for an NMOSFET comparing S_iO_2 and Ta_2O_5 gate dielectric materials.

Simulation

For device fabrication, numerical simulation of processing steps with ***ATHENA*** results in structures which more closely match manufactured devices than is possible using assumptions of ideal processing. The structures produced from process simulation are critical to evaluating device reliability and predicting sensitivity to process variation. For example, the electric field distribution in deep submicron devices at the edges of the drain region determines avalanche breakdown characteristics. Accurate doping profiles, reflecting impurity redistribution following subsequent thermal processing steps, are needed instead of idealized profiles to reveal failure sites within the device. Doping redistribution in the channel region has also been shown to influence short-channel effects. In deep submicron devices, channel carrier quantization possibly violates drift-diffusion physics, and simulation of these quantum effects rely on precise impurity locations.

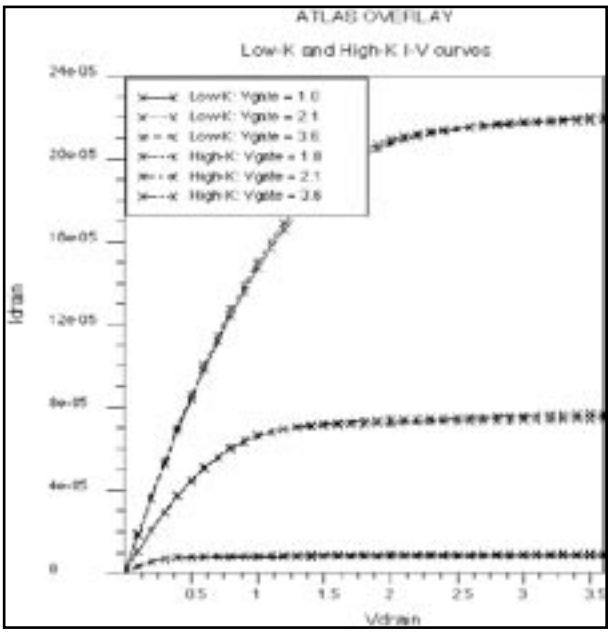

Figure 2. I_D-V_{DS} comparison of high-K gate dieletrics versus conventional processing. The high K material allows equal drive current with a thicker dielectric.

As devices are scaled down to deep submicron dimensions and are operated at frequencies extending into gigahertz, existing circuit models fail to predict capacitive behavior and cannot account for internal heating due to dynamic switching activity. Numerical simulation, particularly RF numerical simulation, is necessary to capture non-isothermal high-frequency switching performance. Scaling also introduces a number of reliability issues not accounted for in traditional transistor models. In devices with an effective channel length approaching 0.1 micron, a gate oxide of under 40 angstroms is required. The device robustness is degraded, since oxide tunneling is increased and defects critically affect the lifespan of the dielectric. To address these shortcomings, new high dielectric constant materials are being considered to provide the same gate capacitance using a thicker material. Device numerical simulation

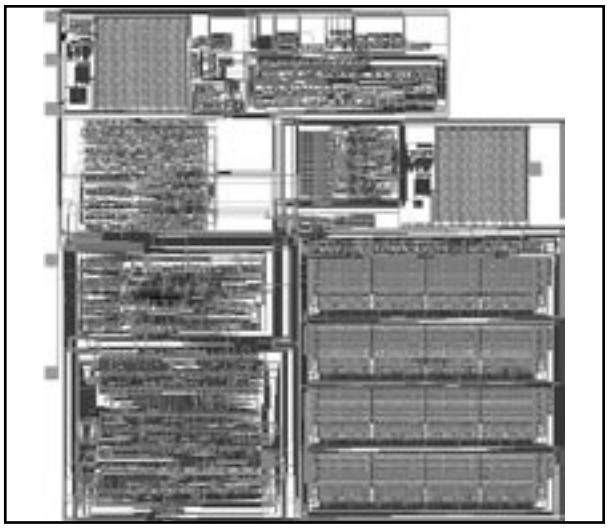

Figure 3. System-on-a-chip layout from UIC.

is required to assess the impact of thin and thick dielectric materials on first-order characteristics like I-V and C-V curves, but more importantly, second-order effects like breakdown and gate control of the inversion layer. Figure 1 shows the structures, created in DevEdit, of an NMOSFET using S_iO_2 and Ta_2O_5, respectively, as a gate dielectric. Simulation results from ***ATLAS***, shown in Figure 2, confirm a match in the I-V curves. Further work is being performed to develop device structures for low- and high-dielectric constant gate oxides for RF applications. ***ATLAS*** is used in optimizing the output characteristics and relate process parameters to specific performance criteria. ***ATLAS*** has been applied previously to evaluate self-heating effects in silicon-on-insulator CMOS [2] and in the modeling of power MOSFETs for RF applications [3].

In designing a complete SOC, analysis of the signal delays and impedances of global and local interconnects is necessary to optimize architectures and circuit topologies. Feature sizes continue to shrink, but as more functions are integrated on-chip the ratio of global routing distances to device dimensions is growing very large. Routing parasitics now dominate over intrinsic device parasitics, and at RF frequencies metallization is more accurately represented by transmission lines instead of lumped or distributed RC networks. To capture layout parasitics, hierarchical simulation of interconnect metallization is needed. Shown in Figure 3 is the UICchip, a 1.2-micron CMOS mixed-signal SOC developed at UIC. It includes a 50-MHz 8-bit microprocessor, 256-byte SRAM, a 400-MHz transceiver, and on-chip power management and regulation of three separate voltage supplies. Simulation of this SOC is challenging due to the interaction of digital and analog blocks which are operated at widely separated frequencies. An essential element in the accurate performance prediction of this project is extraction of device and interconnect parasitics. Logic is affected by increased switching times resulting in conservative estimates of cycle time. Without accurate estimation, analog and RF circuits may suffer from larger non-linearity and inaccurate biasing.

The UIC chip uses a full-custom logic implementation rather than synthesized gates to optimize performance of individual functional units. Silvaco has recently developed a suite of tools for this type of work. **Clever** is being applied to characterize the custom cells and ensure that critical timing margins are met. It is also being used to relate layout topography to specific RF performance metrics, to identify which layout geometries can optimize linearity and noise. To validate parasitic values extracted through simulation, fabricated test structures are required which characterize the resistance and capacitive coupling of multilevel interconnects. On-wafer measurements of these test structures will be compared with **Exact** simulations of identical structures. **Exact** can also be used to determine the range in interconnect parasitics due to process variations, essential in applying statistical process control to yield. Finally, at the chip-level, ***HIPEX*** extraction of all layout parasitics can be performed to compare the accuracy of hierarchical modeling with traditional flat lumped-element models. A significant feature of ***HIPEX*** is its interface to numerical simulation of complex regions.

Conclusions

In developing technologies and ICs for mixed-signal systems-on-a-chip, numerical simulation from the process to the IC layout parasitic extraction is needed to capture important second-order effects which critically impact reliability and performance. Digital systems cannot be approximated by simple switch-level simulations, and time- and frequency-domain simulation is required to analyze the fundamental analog nature of these circuits. For RF circuits, detailed device level simulation is necessary to optimize the internal structure for noise performance, linearity, and distortion. This type of optimization cannot be performed by assuming an equivalent circuit model. In designing for highest performance and lowest power, interconnect parasitics must be determined with a high degree of accuracy early in the design phase. The ***DISCOVERY*** tool suite is particularly well-suited for determining chip-scale device and interconnect parasitics. Its interfaces with numerical simulation of processes and devices are necessary in developing the on-chip matching networks that will emerge in SOCs operating at high frequency and low power.

References

[1] K. Shenai, E. McShane, and M. Trivedi, "Electronics Technologies for Intelligent Transportation Systems," in IEEE Conference on Intelligent Transportation Systems (ITSC), November 1997.

[2] D. A. Dallmann and K. Shenai, "Evaluation of Self-Heating in SOI CMOS ULSI," Int'l Integrated Reliability Workshop Final Report, pp. 83-89, October 1994.

[3] P. Perugupalli, M. Trivedi, K. Shenai, and S. K. Leong, "Modeling and Characterization of 80V LDMOSFET for RF Communications," in Proceedings of Bipolar Circuits and Technology Meeting (BCTM), pp. 92-95, September 1997.

Calibrating Reverse Short Channel Effects in MOSFETs

Introduction

This article focuses on the effects of process and modeling parameters on device electrical characteristics and uses the threshold voltage versus gate length of a n-MOSFET as an illustration. It has long been the adage of experienced TCAD users that the correct modeling of the process flow should represent approximately 90% of the effort, the remaining effort being directed towards electrical device modeling. In other words, if the process flow is correctly modeled, the basic electrical characteristics will be largely correct. This truism is based on the fact that device physics is well understood and most values required for device modeling are well known for silicon. These device modeling parameters are included as the default values in **ATLAS.**

Modeling Short Channel Effects

The Short Channel Effect (SCE) and Reverse Short Channel Effect (RSCE) are strongly affected by changes in the process flow and are caused primarily by implant induced defect enhanced diffusion. These effects therefore present themselves as ideal candidates for tuning implant damage models in ***ATHENA*.**

The short channel effect is universal in MOSFETs and represents the gradual shorting together of the source and drain diffusions as the gate length reduces to low values. This one effect allows calibration of two phenomenon, namely the lateral spread of the as-implanted source-drain dopant profiles, and the effects of subsequent diffusion steps.

The reverse short channel effect only occurs when the peak of the channel implant, usually boron, lies below the silicon-SiO2 interface in the centre of a long channel MOSFET. Enhanced diffusion, caused by lateral implant damage to the source-drain area, moves the peak concentration of boron closer to the surface in these regions. For short channel MOSFETs, therefore, a higher percentage of the channel has a higher concentration of boron at the surface than for long channel devices. Short channel devices therefore have a higher threshold voltage than long channel devices until the channel becomes so short that the usual short channel effect takes over. The reverse short channel effect therefore allows the calibration of defect production and annealing effects in both the bulk of the silicon and at the gate oxide interface where the interface acts as a sink for defects. Appropriate models for these physical effects should be enabled in ATHENA before the source/drain implantation:

```
METHOD  FULL.CPL  CLUSTER.DAM  HIGH.CONC
```

Parameter Tuning

ATHENA allows user definable damage and anneal factors for accurate tailoring of process models resulting in good predictability for the final device. For a given channel implant dose and energy, the magnitude of the peak value of reverse short channel threshold voltage will be strongly related to the magnitude of the initial implant damage. The implant damage factor can be adjusted by specifying the CLUST.FACT parameter. The effect of adjusting the CLUST.FACT parameter for an otherwise fixed typical process flow, is shown in Figure 1. Initial experiments have suggested a value of 1.4 to be approximately correct.

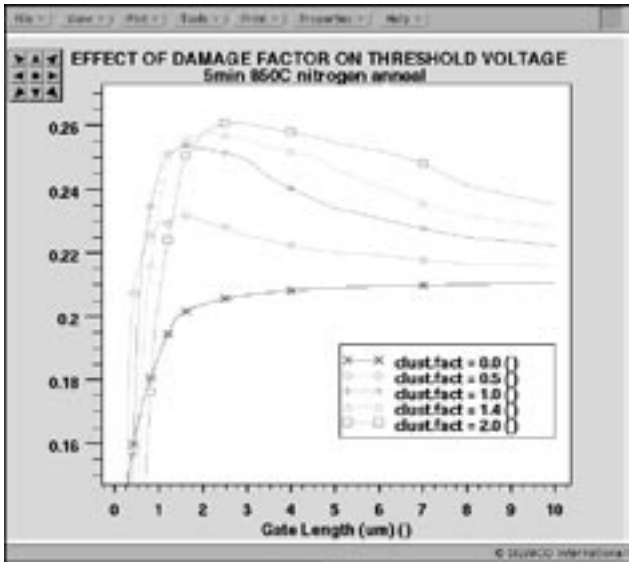

Figure 1. Showing the effect of changing the CLUST.FACT damage factor in ***ATHENA*.**

The important role of damage in determining threshold voltage is clearly demonstrated in Figure 1. The importance of correctly modeling the damage in ***ATHENA*** is also indicated, since the large range in the results was obtained by changing just the implant damage factor CLUST.FACT in ***ATHENA*.** If the process flow has been accurately modeled, calibrating the correct damage factor to a particular process is merely a question of matching the correct magnitude of change in the peak threshold voltage. Thus, one parameter has now been calibrated.

The correct rate of interstitial dissipation at the silicon-gate oxide interface can also be calibrated using this plot. The rate of roll-off of threshold voltage with increasing gate length is a result of how far interstitials generated during the source-drain implants can diffuse before being dissipated at the surface. The tuning parameter associated with surface interstitial dissipation is KSURF.0. A higher value of KSURF.0 will give rise to a greater roll-off in threshold voltage with gate length. This parameter can also therefore be unambiguously calibrated to a particular process.

Finally, the rate of roll off for very short gate lengths is a result of how much lateral dopant spread occurred during implantation and subsequent diffusion. Since

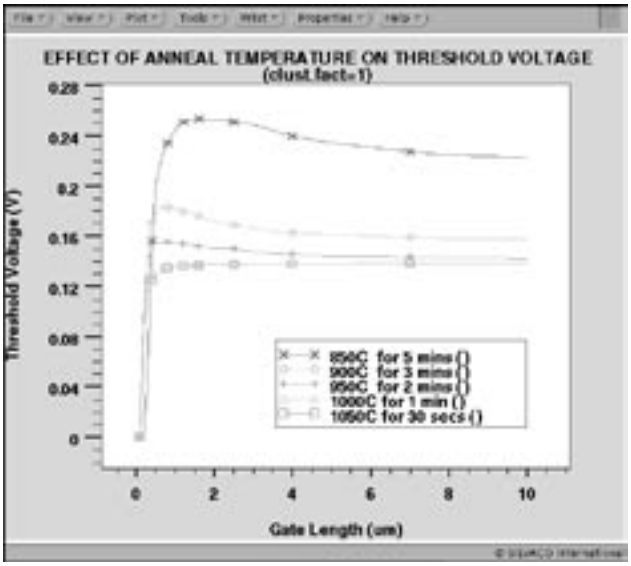

Figure 2. Showing the effect of anneal conditions on the threshold voltage of a MOSFET.

the annealing steps in the process are known, the only variable to tune is the implant lateral spread parameter. This parameter is called `LAT.RATIO1` in ***ATHENA***.

To conclude this brief summary on tuning ***ATHENA*** for MOSFETs, it has been shown that using just one set of measured data, namely a plot of threshold voltage variation with gate length, three of the most important parameters in ***ATHENA*** can be unambiguously tuned to their correct values. To confirm calibration of the process simulation, the user should perform additional device simulations and compare these results to measured data not used in process calibration. Typically, this could be similar data with a substrate bias. It is crucially important that the user has used appropriate models in the process simulation before turning to tuning parameters. This includes the models `CLUSTER.DAM`, `FULL.CPL` and `HIGH.CONC` in the `METHOD` statement *before* implantation statements where the dose exceeds approximately 1e13/cm^2 and the model `TWO.DIM` for oxidations and implantations less than 1e13/cm^2. The FERMI model should only be used where no oxidation or implantation damage has occurred.

Process Parameter Effects

This section shows the effects of changing actual process parameters on the electrical results of a typical MOSFET process flow. In this article, the effect of activation anneal temperature has been chosen as a process variable. This particular parameter was chosen because the effect of variations in activation anneal temperature are the opposite of what would be expected intuitively. Specifically the lower the anneal temperature, the greater the dopant diffusion becomes. To understand this phenomenon, accurate modeling of defect diffusion is key. The high rate of dopant diffusion for low temperature anneals is a particular problem for sub-micron radiation hardened devices, where anneals above 850^{o}C0 have to be avoided.

Figure 2 shows a set of modeling experiments where the `CLUST.FACT` parameter has been fixed, while the anneal temperature / time parameters are the variables. The minimum time for a low temperature anneal is limited by the rate of damage removal. There is little point in using a short activation anneal at 850C for example, since the material would still be so damaged that the device electrical characteristics would be very poor.

For the low temperature anneals, an anneal time as short as possible was chosen, consistent with a significant amount of damage removal; whilst the high temperature anneals are, if anything, longer than required. The modeled effects are therefore understated. Figure 2 shows that for the two highest temperature anneals (1000 and 1050^{o}C), the dopant has almost not moved at all to the extent that the reverse short channel effect (RSCE) is non existent and the short channel effect (SCE) occurs for shorter channel lengths. As the anneal temperature reduces to 850C, the high dopant diffusion effects such as RSCE and SCE become greatly enhanced.

The understanding of this counter-intuitive result relies on the realization that two competing physical effects occur at the same time during an activation anneal and each effect has a significantly different temperature coefficient. These two effects are:

- defect enhanced diffusion
- defect annealing

In effect what happens at the two extremes of anneal temperature is as follows: for low temperature anneals, the defects are almost insoluble and remain in the silicon for very long times. The huge increase in diffusion rate for defected material (approximately x1000) therefore results in the dopant diffusing large distances before the defects are dissolved. For the high temperature anneals, all the defects are dissolved in a very short time, so almost no defect enhanced diffusion occurs. For the remainder of the high temperature anneal, therefore, only intrinsic diffusion takes place which is approximately one thousand times slower. An important result of this is that for high temperature anneals *most of the diffusion takes place during the temperature ramp-up phase*, even for rapid thermal anneals. It is therefore vitally important to include the temperature ramp-up of the first heat cycle after heavy implants during the process simulation. The ramp down is much less important.

Summary for MOS Simulations

Measured data for Vt versus length is an invaluable aid for tuning purposes. Defect damage during implantation and defect combination coefficients can be tuned to this curve. Since diffusion temperature after heavy dose implants is a key variable in determining any SCE or RSCE, it is important to include the ramp-up steps of final diffusion cycles.

Calendar of Events

May

1
2
3
4
5
6
7
8
9
10
11
12 CICC - Santa Clara, CA
13 CICC - Santa Clara, CA
W/S - Guildford, UK
14
15
16
17
18
19
20 W/S - Guildford, UK
21
22
23
24
25
26
27 W/S - Scottsdale, AZ
W/S - Munich, Germany
28 W/S - Scottsdale, AZ
30
31

June

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15 DAC 98 - San Francisco, CA
16 DAC 98 - San Francisco, CA
17 DAC 98 - San Francisco, CA
W/S - Munich, Germany
18
19
20
21
22
23
24 W/S - Grenoble, France
W/S - UCLA, Los Angeles, CA
25 W/S - UCLA, Los Angeles, CA
26
27
28
29
30 W/S - Guildford, UK

Bulletin Board

New Release of CLEVER

Silvaco International will announce at the DAC '98 trade show an update to the industry's first TCAD-driven, cell-based, parasitic-extraction program. ***CLEVER*** models the entire cell structure in 3-D, therefore reducing development time by allowing designers to accurately determine the complete cell parasitics.

CLEVER uses physically based lithography, deposition, etch and oxidation models to accurately simulate the true 3-D geometry of a cell as manufactured. An efficient filed solver is applied to generate a fully back-annotated SPICE netlist of the cell.

Year 2000 Compliance

Silvaco's software has been upgraded and thoroughly tested to ensure year 2000 compliance.

- All of our software now use four digit year numbers such as "1997" not just "97". This is where other software providers may have difficulty with year 2000 compliance.
- Our proprietary license manger (Silvaco Floating License Manger) which is responsible for managing our licenses also uses the four digit year numbers.
- All licenses that have been purchased by customers are valid past the year 2000. These licenses have an expiry date of 31:Dec:2099.

See Silvaco at San Francisco DAC '98

Silvaco will be exhibiting the latest in TCAD Driven CAD tools at the Design Automation Conference. The exhibition will be 15-17th June at the Moscone Center, San Francisco. Silvaco will present the latest advances in:

- SmartSpice
- NT-based Layout and Verification Tools
- Technology based Parasitic Extraction
- 3D TCAD

For more information on any of our workshops, please check our web site at ***http://www.silvaco.com***

Hints, Tips and Solutions

Andy Strachan, Applications and Support Manager

Using Clever to Simulate the Effect of Lithographic Misalignment of Metal Via Resistance

To meet the requirements on metal pitch and number of metal layers for sub-0.25um designs, the process technology for the metalization layers has become more complex. Modern process flows are using copper interconnect, damascene processing, low-k dielectrics and CMP to aid miniaturization and improve interconnect parasitics.

Clever is an interconnect simulator based on 3D process simulation. As such it is able to aid process developers by allowing them to study various process effects on interconnect geometry and parasitics. Models in **Clever** include etch, deposition, oxidation and lithography which allow realistic simulation of the as-manufactured geometries of interconnect structures. Although **Clever** can be applied to large structures for complete cell characterization it is also possible to use **Clever** to examine individual process effects.

For sub-0.25μm geometries the process margins will become much more important. The tolerances on line width due to lithography and etch variations may not scale directly with the nominal line width.

The measured effect of misalignment in photolithography between a top metal line and a bottom metal line with via for different metal processes has been reported in [1].

Clever was applied to this situation to simulate the photolithography effects such as corner rounding and line shortening. In addition various misalignments were specified between the top metal line and the underlying structure. Mask misalignments in **Clever** can be modeled by using the X/Y misalignment option on the DEFINE/LAYERS menu in **MaskViews** or through a syntax option on the `MASK` statement. After the process simulation is completed, **Clever** extracts the resistance of each structure. A results summary as a function of amount of misalignment is presented in Figure 1.

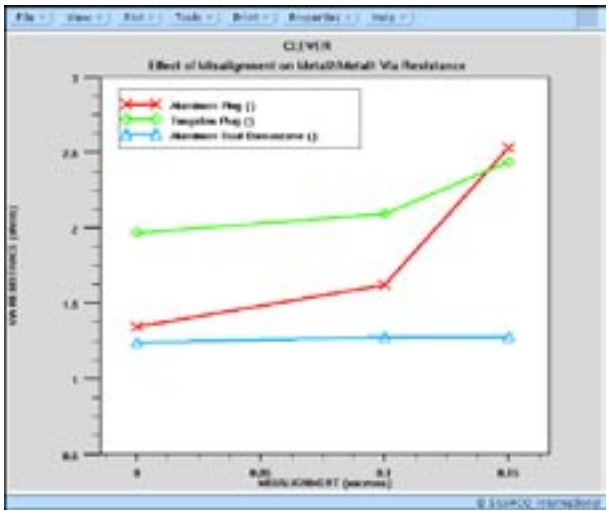

Figure 1. Change in via resistance as a function of photo misalignment for various process. Dual damascene processing is less sensitive to misalignment.

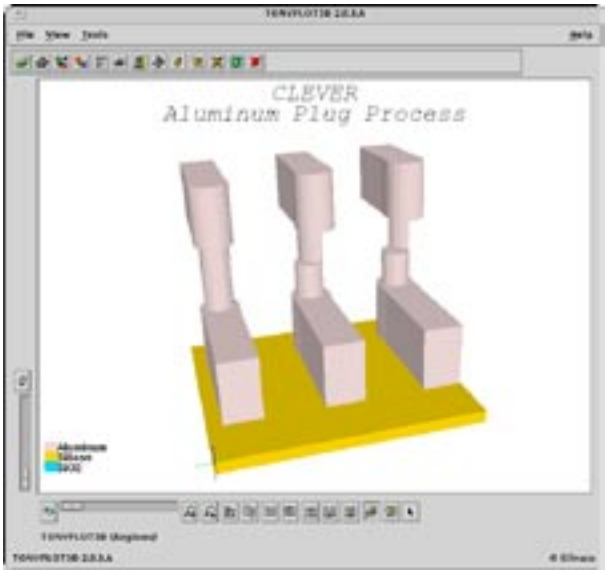

Figure 2. Geometry of Al plug process with from left to right, zero, 0.1 µm and 0.15 µm misalignment of the metal 2 layer.

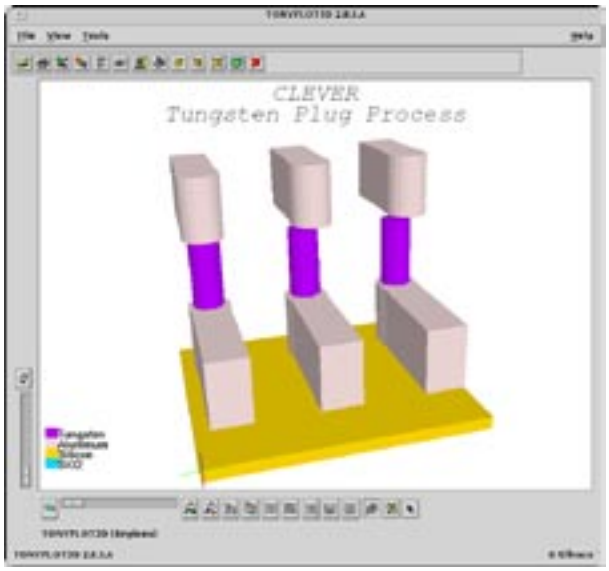

Figure 3. As figure 2, but for a Tungsten plug process.

Simulations were done for an Aluminum plug process shown in Figure 2. The misalignment causes part of the metal in the plug to be removed causing increased contact resistance and potential electromigration problems. The tungsten plug process shown in Figure 3 shows a similar reduction in the metal2/via contact area. This leads to increased contact resistance although, since the resistance is dominated by the lower conductivity tungsten, it is not so large an effect.

A dual damascene process similar to [1] was modeled and shown in Figure 4. In this process the metal2 and via are filled by the same metal deposition step. In fact the misalignment *increases* the contact area. The resistance of the structure remains constant over the range of misalignment considered conforming the measured results. The paper also reports that time to electromigration failure is improved with increasing misalignment. **Clever** is capable of modeling the advanced interconnect processes currently being developed. It can examine process effects on parasitics and help with definition of suitable process margins based on parasitic analysis. The effect of such process changes can be characterized on small structures as presented here. However it is possible to extend the simulations to model complete cells including process variations to generate worst-case or corner characterizations for cells.

References

[1] "Comparative Study of W-plug, Al-plug and Al-Dual Damascene for 0.18um ULSI Multilevel Interconnect Technologies", Kikuta et al (NEC), International Interconnect Technology Conference 1998, p140.

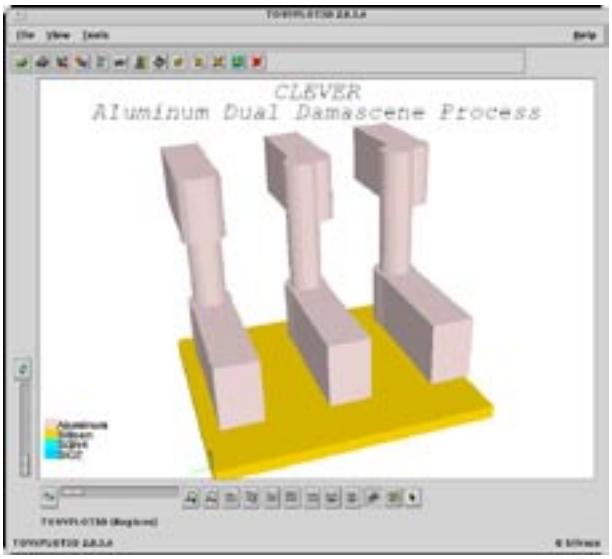

Figure 4. As figure 2, but for Al dual-damascene process. Note the increase in contact area with misalignment.

Call for Questions

If you have hints, tips, solutions or questions to contribute, please contact our Applications and Support Department

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Hints, Tips and Solutions Archive

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...continued from page 2.

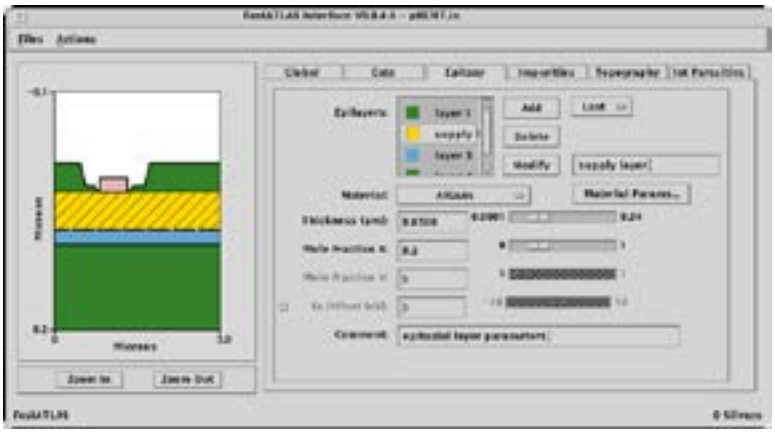

Figure 6. The ***FastBlaze*** GUI is called from ***DeckBuild*** and allows easy definition of complex III-V FET structures for FastBlaze.

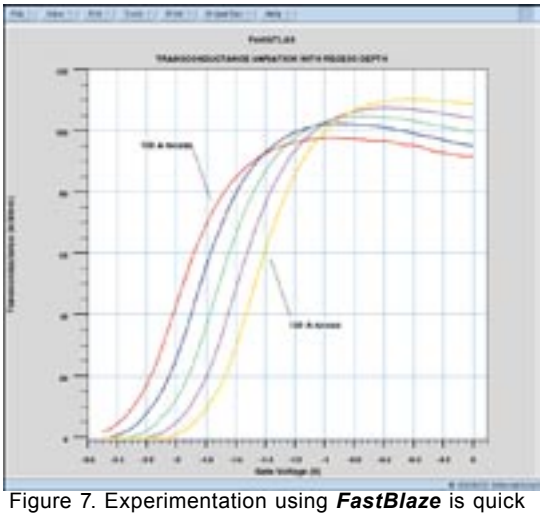

Figure 7. Experimentation using ***FastBlaze*** is quick and simple. Here the transconductance is shown as a function or recess depth.

Summary

FastBlaze brings together sophisticated device physics tuned using Monte Carlo simulation with user-oriented operation. The solution techniques used allow most simulations of I-V families or RF characteristics to be run in less than 1 minute. This means that experimentation with device structures can be run much more efficiently and accurately than in conventional device simulation or circuit simulators.

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