Simulation Standard

TCAD Driven CAD

A Journal for Process and Device Engineers

3D Simulation of Power Devices using *Giga3D* and *MixedMode3D*

Introduction

Recent additions to the ***ATLAS*** device simulation framework have added the ability to simulate 3D electrothermal effects in ***Giga3D*** and mixed circuit simulation with 3D device simulation in ***MixedMode3D.*** The new modules add to the existing 3D device simulation within ***ATLAS*** as shown in Figure 1. They show the migration of existing 2D device simulation models and techniques to a full 3D approach. ***ATLAS*** currently supports 3D simulation of most common device technologies:

Device3D	- MOS, Bipolar, EEPROMs
Blaze3D	- MESFETs, HEMTs, HBTs
Giga3D	- power devices, SOI, ESD effects
MixedMode3D	- power devices embedded in circuitry , ESD effects, latchup
TFT3D	- thin film transistors
Thermal3D	-thermal effects in packaging
Quantum3D	- quantum moments solver

The new modules ***Giga3D*** and ***MixedMode3D*** can be used with both ***Device3D*** and ***Blaze3D*** to model silicon and non-silicon technologies respectively.

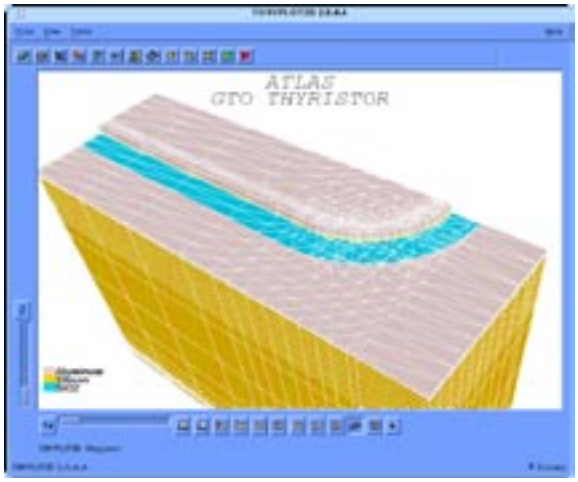

Figure 2. GTO thyristor geometry. This device can only be simulated correctly in 3D.

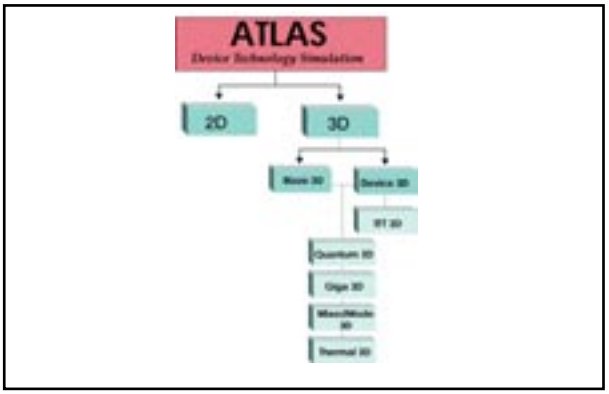

Figure 1. 3D device simulation within ***ATLAS***.

2D Versus 3D Simulation

For many devices 2D ***ATLAS*** simulation has been sufficient to describe the device behavior to the limit of simulation accuracy. Using 3D simulations will always be at least an order of magnitude slower than 2D and have more limitations on the accuracy of the initial structure definition.

However in many technologies the device physics requires a 3D approach to simulation. Examples include substrate contacts in SOI, current crowding in power device structures, width effects in FETs. In addition for ***Giga3D,*** current filimentation is essentially a cylindrically symmetric event for which full 3D electrothermal device simulation is required.

Defining Devices for *Giga3D*

Accuracy in definition the initial structure for 3D device simulations can often be the limiting factor in overall

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INSIDE

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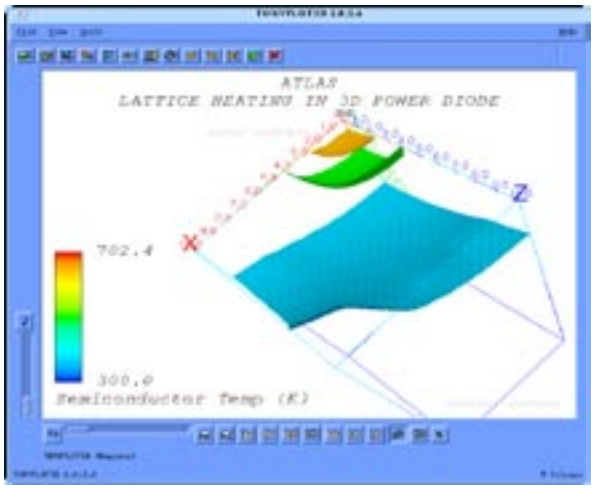

Figure 3. Isosurfaces of temperature in a power diode with current crowding into the anode.

simulation reliability. ***ATLAS*** accepts 3D structures defined either using the ***ATLAS*** syntax or from ***DevEdit3D***. The familiar ***ATLAS*** syntax has been extended to support objects in the z-direction. This includes the `THERMCONTACT` definition required in ***Giga3D.***

DevEdit3D can be used as an interactive or batch mode tool to pre-process a 3D device structure. It accepts input from ***ATHENA***, ***SSuprem3*** or ASCII doping profiles. It also allows arbitrary device structures including structures with circular masks.

Defining a Netlist for *MixedMode3D*

The SPICE-like netlist used in ***MixedMode3D*** is defined between `.BEGIN` and `.END` statements in an ***ATLAS*** input file. Circuit simulation primitives are defined in the standard SPICE manner: D for diodes, Q for bipolars, L for inductors. Circuit elements to be simulated by device simulation are given the identifier 'A'. A typical netlist might include:

```
AIGBT 1=gate 2=emitter 4=collector inf=myigbt.str
```

Node numbers from the circuit are paired with electrode names from the ***ATLAS*** device on the 'A' line.

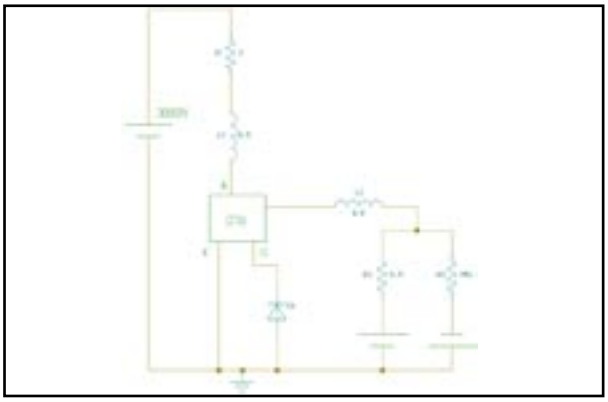

Figure 4. Circuit schematic for a GTO thyristor. The GTO element is simulated using 3D device simulation.

Power Device Simulation Example

Currently power device simulation engineers have been applying Silvaco's ***MixedMode*** simulator to good effect. By coupling together a spice circuit with 2D device simulations of the power device, much information about device performance has been obtained. However, this has neglected three important aspects of the physical device operation

- current filamentation occurs in a localized 3D region
- heat generation is 3D
- 3D boundary conditions

Figure 2 illustrates a GTO thyristor device which may exhibit all three of these problems. The GTO device has been designed with a forward blocking voltage of 3500V. To model the operation of this device in practice we have embedded the GTO thyristor into a circuit shown in Figure 4. ***MixedMode3D*** simulation of this circuit produces the result shown in Figure 5. This circuit response can be explained as follows. The GTO thyristor is initially driven into the ON state by increasing the gate current to 2.1A and the supply voltage to 3000V. The closure of a switch is then modeled by forcing the resistor R3 to change from 1Mohm to 1mohm in only 100ns. This results in the gate turning off the device and the anode current falling to zero. However, the high negative dI/dt in the load circuit results in a large positive voltage in the load inductor L1. This produces an over-voltage on the anode contact of the GTO and causes the voltage to exceed 3000V. The over-voltage may cause the device to exceed its forward blocking voltage, causing impact ionization to occur, and as a result the turn-off of the GTO will be affected. Accurate ***MixedMode3D*** simulation is vital in order to properly characterize these effects.

Conclusion

The addition of ***Giga3D*** and ***MixedMode3D*** to ***ATLAS*** allows users to perform full 3D simulations of electrothermal device behavior. For power device applications the combination with ***MixedMode3D*** is particularly powerful to model the switching of devices within a circuit environment.

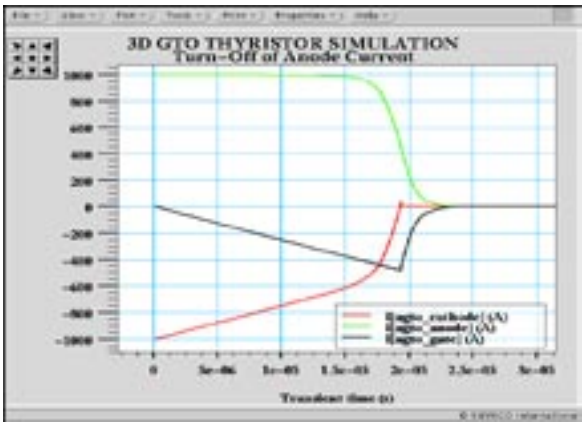

Figure 5. Currents in the GTO thyristor during turn-off through external circuit.

MixedMode Simulation of Power Electronic Converters

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Introduction

With mounting concern for energy conservation and nature preservation, power electronics is becoming increasingly dominant in everyday life. Power electronics systems have proliferated to a wide range of applications from telecommunications and information processing to medicine and transportation. Radical developments in power semiconductor devices have been instrumental in this power electronics revolution.

In order to push the technology further, new device structures and process technologies are rapidly being developed. Complexity of these device structures and processes hinders a full understanding of device operation based on the structural information alone. Improper understanding hampers the development of reliable circuit models of these circuits. It is essential to understand internal carrier dynamics for optimum utilization of a high power device.

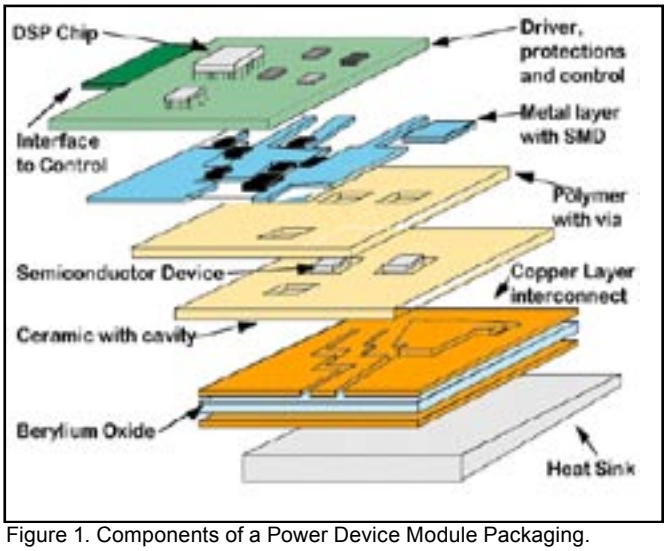

Figure 1. Components of a Power Device Module Packaging.

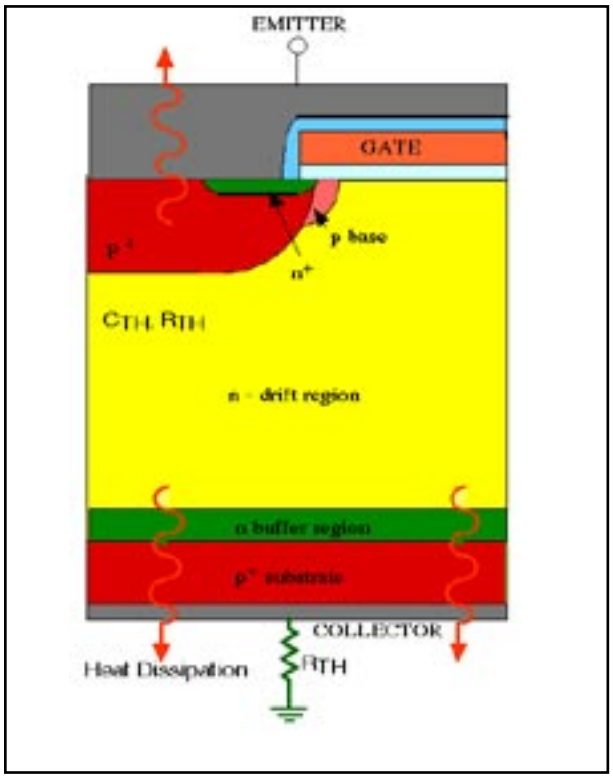

Figure 2. Two-dimensional representation of Insulated Gate Bipolar Transistor along with thermal resistance at collector electrode.

Power semiconductor devices are mostly used in applications that subject them to high stress conditions. Some such conditions include short circuit and inductive load turn-off. The device has to conduct rated current with bus voltage across its terminals in such conditions. Large power dissipation results in considerable heat generation within the device. Thermal considerations can seriously compromise device reliability, and, in fact, limit the Safe Operating Area (SOA) of the device at the high-voltage, high-current limit. Efficient heat dissipation becomes an important issue as the power device module becomes more complex to cater to a greater demand for application specific system solution. Various layers in a typical Application-Specific Power Electronics Module (ASPEM) are shown in Figure 1. Heat generated within the device diffuses through the semiconductor and various packaging layers before being dissipated in the ambient. Thermal resistance of the package should be very low to facilitate better heat dissipation. Further, the wire bonds may fail at high temperature levels. A better understanding of electrothermal performance of the device will lead to development of more reliable devices and more efficient package designs.

Traditionally, device optimization involves running split-lots in a wafer fab, and measuring the electrical characteristics of prototype devices. This is a very expensive and time-consuming venture, especially so as wafer sizes increase and processing equipment becomes

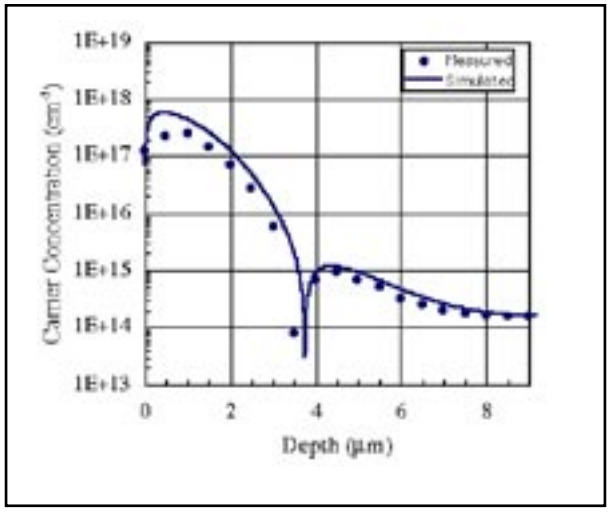

Figure 3. Measured and simulated doping profile of the p-base of IGBT.

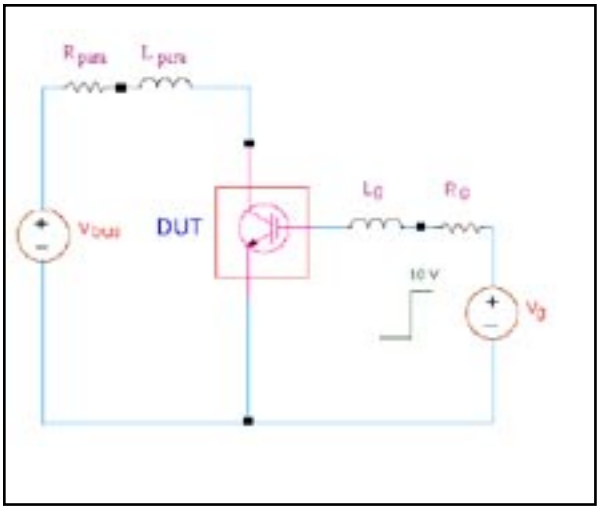

Figure 4. Test circuit used for short-circut switching study.

more expensive. Two-dimensional numerical simulators are emerging as invaluable tools towards a better understanding of semiconductor device dynamics under actual circuit conditions [1]. By solving semiconductor equations at each point within a 2-D representation of the device, under boundary conditions imposed by external circuit elements, 2-D simulators provide direct access to internal device parameters. This enables optimization of device carrier dynamics in an actual circuit application environment. Electrothermal simulations can be performed to incorporate effects of self-heating that results from power dissipation within the device. Package influence can be accounted for by connecting thermal resistance of various layers, as depicted in Figure 2 for an Insulated Gate Bipolar Transistor.

Simulation of Power Converters

In this paper, the importance of mixed-mode simulations is demonstrated in the study of Safe Operating Area of Insulated Gate Bipolar Transistors (IGBT) [2]. The cross-section of the device, shown in Figure 2, was created from the process flow using the two-dimensional process simulator ***ATHENA*** [3]. The device is rated 600 V, 50 A. Simulated doping profile of the p-base is compared with SRP data in Figure 3, revealing a very close match between the two doping profiles. Effective area and lifetime of the device were determined to obtain a good match with measured static characteristics. Matching of static characteristic was done using the 2-D device simulator, ***S-Pisces*** [4].

The structure generated was then used in the mixed device and circuit simulator, ***MixedMode***[4], to perform electrothermal simulation of short circuit performance of the device. In many power conversion applications, short circuit condition is a frequently occurring fault. Ability of the power device to withstand short circuit conditions is an important requirement. The test circuit used for the study is shown in Figure 4. Influence of the package is accounted for by attaching thermal resistance of various packaging layers at the device electrodes. Thermal boundary conditions were applied by maintaining the device electrodes at an ambient temperature of 400 K. Performance of the device under short circuit stress of 10μs is shown in Figure 5. When the device is turned on initially, current increases rapidly, but then starts drooping. This results from mobility reduction due to temperature rise. The device successfully turns-off after 10μs of stress. Extended exposure of the device to this condition eventually leads to device failure, as shown in Figure 5, by the dashed lines. After breakdown, device current rises rapidly and uncontrollably, while voltage falls down [5].

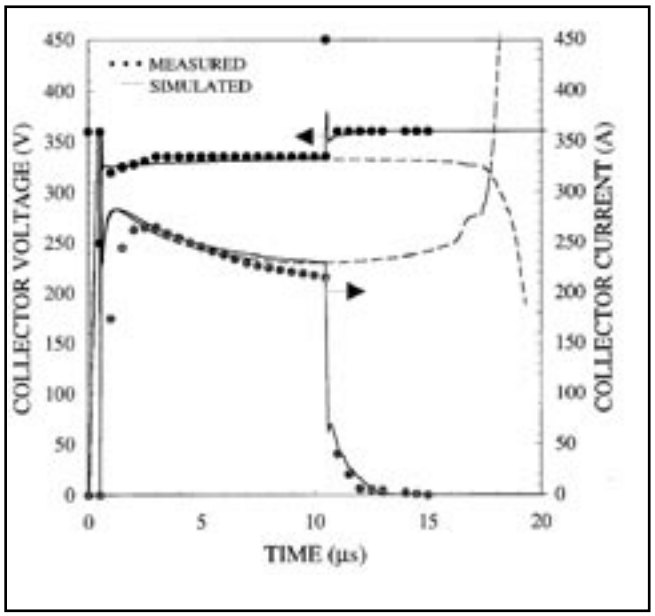

Figure 5. Measured and simulated short circuit performance of IGBT.

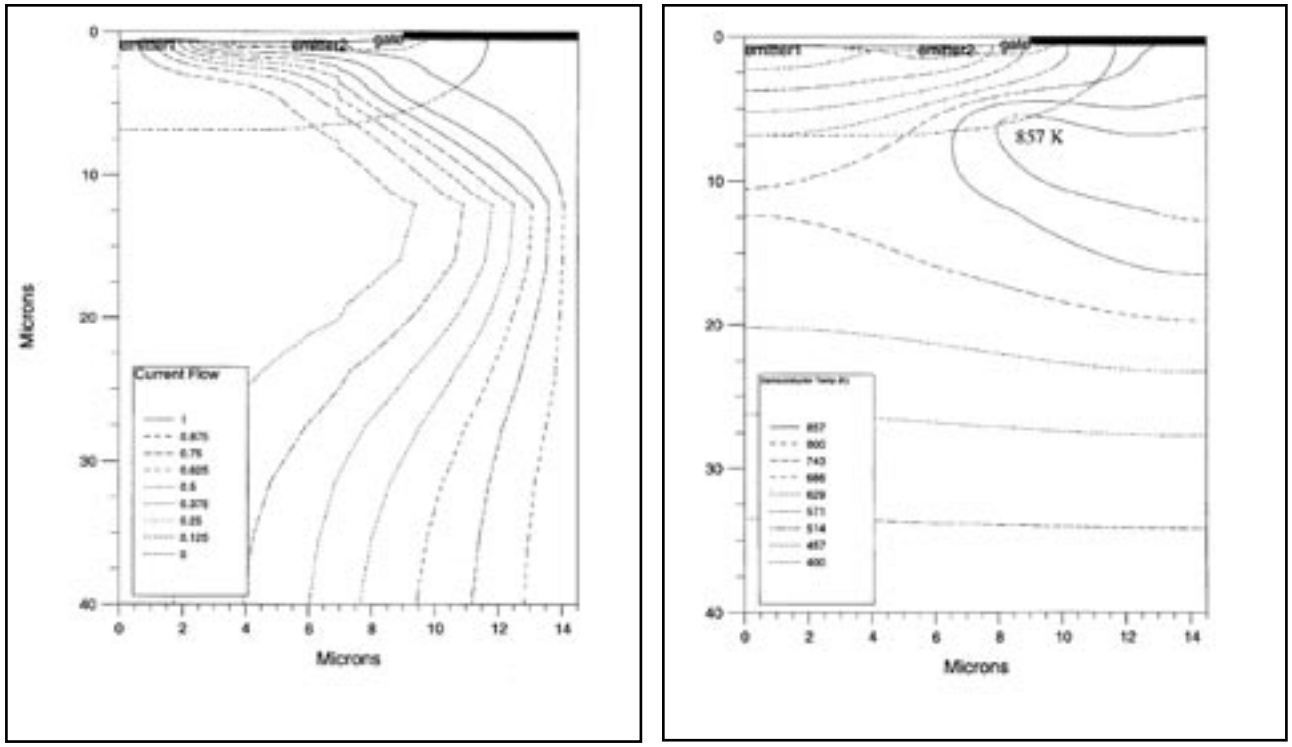

Figure 6. (left) Current flowlines, and (right) temperature distribution within the device at short circuit failure.

Figure 6 depicts the current flowlines and temperature distribution within the semiconductor for the device conducting in breakdown condition. As can be seen in Figure 6, current flowlines are concentrated at the curvature of the p-base n-drift region junction. Maximum temperature within the device is localized in the same region, as shown in Figure 6. the reverse biased p-base n-drift region supports the entire applied voltage leading to a significant electric field. High current density through the region leads to significant power dissipation and temperature rise. At higher temperatures, there is an increased availability of carriers. This leads to a further increase in the impact generation rate in the high field region. Impact generation in this region and temperature rise initiate a regenerative process and the device finally breaks down due to thermal instability [5]. Location of the hot spot was confirmed experimentally using IR imaging techniques.

With an understanding of the physical phenomena governing the observed characteristics, mixed device and circuit simulations can be used to make changes in actual process and device design parameters. These changes can significantly impact both performance and Safe Operating Area (SOA) of the device. Important trade-off among performance and SOA parameters can be identified, and traded-off using the ***ATHENA*** and **ATLAS** frameworks at process and device level.

Conclusion

As power semiconductor devices find more widespread and multifarious use in industry, it is becoming important to design and optimize the devices at the application level. Mixed device and circuit simulations offer an economical, feasible and competitive alternative to running several split lots in the wafer fab for application-specific optimization of devices. ***ATHENA*** and ***ATLAS*** frameworks have been successfully used in this work to study the short circuit failure of IGBTs. Electrothermal simulations allow study of the effect of self heating on circuit performance of the device. The simulator also incorporates electrical and thermal package parasitics.

References

[1] K. Shenai, "Mixed-mode circuit simulation: an emerging CAD tool for the design and optimization of power semiconductor devices and circuits," IEEE 1994 PELS Workshop on Computers in Power Electronics, 1994, pp. 11-15

[2] M. Trivedi and K. Shenai, "Mixed-mode simulations for power system optimization," 21st Intl. Conf. on Microelectronics, 1997, pp. 451-458

[3] ATHENA Users Manual, Silvaco International, Santa Clara

[4] ATLAS Users Manual, Silvaco International, Santa Clara

[5] M. Trivedi and K. Shenai, "Investigation of the Short-Circuit Performance of IGBTs," IEEE Trans. Electron Devices, vol 45, no. 1, pp. 313-320, 1998.

Polysilicon Gate Depletion Effects in Sub-Micron MOSFETs

It is usually assumed that the poly gate in a MOSFET is doped at a concentration such that depletion in the gate either does not occur or that any depletion effects can safely be ignored. This article aims to quantify poly depletion effects for typical sub-micron device dimensions using ***ATHENA*** and ***ATLAS*** process and device simulators. The simulations show that the resultant effect on electrical characteristics often *cannot* be ignored.

These simulations show the importance of *not* defining the poly gate itself as the electrode when simulating MOSFETs. This would instruct the simulator to treat the poly-gate as a perfect conductor which would by definition not deplete. The accurate approach is to deposit metal onto the poly and define this metal layer as the electrode. This second approach has an added advantage in that it eliminates the need for the user to estimate the polysilicon work function since **ATLAS** can now calculate the actual workfunction from the doping profile. In a typical device the doping concentration in the poly at the end of processing can often yield a work function that differs significantly from the ideal case, resulting in shifted MOS electrical characteristics.

Modern Processing Techniques that Reduce Poly Doping.

A number of processing techniques currently used can reduce poly doping from the ideal saturated value. Some of the more common ones are discussed below.

(i) Silicide suck-out effects

The almost universally used silicide techniques for reducing poly and source-drain resistance have one slight disadvantage in that the process of forming the silicide "sucks out" a significant proportion of the dopant in the poly. The effect this has on device characteristics depends on how much dopant was in the poly prior to silicide formation.

(ii) Insufficient Implant Dose

In earlier technologies, the poly was doped in-situ as it was deposited, allowing total saturation of the poly with dopant. The effects of silicide "suck out" discussed above were therefore dramatically reduced. In modern processes, however, the in-situ method has been replaced with the deposition of nominally undoped poly, which is then implanted. Often the total implanted dose is significantly less than the total dose achieved with in-situ methods, enhancing the effects of silicide dopant reduction.

(iii) Compensation from P+ Implant

It is common practice, although not universal, to perform an unmasked P+ source-drain implant. This relies on the N+ poly doping being of significantly higher doping concentration, such that it remains N+ after being effectively partially compensated by the P+ implant. The P+ implant can reduce the effective N+ doping concentration in the poly quite significantly. In many processes P+ compensation changes the work function of the gate.

(iv) Dopant Evaporation

The activation anneal can result in significant evaporation of dopant, especially arsenic. The evaporation effect is correctly modeled in ***ATHENA***. However, in order to accurately model dopant evaporation, the simulator input deck must be realistic. If the real device has a thin film of native oxide on the poly prior to the activation anneal, this will significantly reduce dopant evaporation. Be sure to deposit or grow the correct thickness of poly native oxide in ***ATHENA*** prior to the activation anneal for accurate simulation of the effect.

The Effects of Reduced Poly Doping

There are several effects of reduced doping in the poly that result in non-ideal electrical behavior in the final device. The main points are discussed below.

(a) the poly-silicon work function is increased from a near ideal value of 4.17eV achieved using in-situ poly doping to a more typical value of approximately 4.3 to 4.4eV for implanted/P+ compensated poly gates.

(b) the poly can become depleted during normal device operation. The resultant voltage drop will cause a loss of current drive in the final device.

(c) depletion in the poly can give rise to inaccurate measurement of oxide thickness if C-V curves are the source of the measurement. The effect is enhanced for thinner gate oxides. A further reduction in accuracy from C-V measurement originates from the quantum nature of the inversion region itself. In essence, the peak concentration of carriers in an accumulated device resides further away from the interface than is predicted by classical physics. This effect enhances the reduced capacitance measured, compounding the derived oxide thickness error.

Quantum effects are modeled in **ATLAS** and are activated by including the parameter `QUANTUM` in the `MODELS` statement.

Using ATHENA and ATLAS to Investigate the Effects of Poly Doping

The basic effects of poly doping can be simulated quickly and simply in 1D using typical Vt implant doses and energies. For investigation of poly depletion effects that occur whilst the device itself is inverted, the poly and channel doping are required to be of the same type. ie. N+ poly with n-type channel (the situation for a p-channel device) or P+ poly with a p-type channel. For similar levels of doping, the effects will be the same in either case.

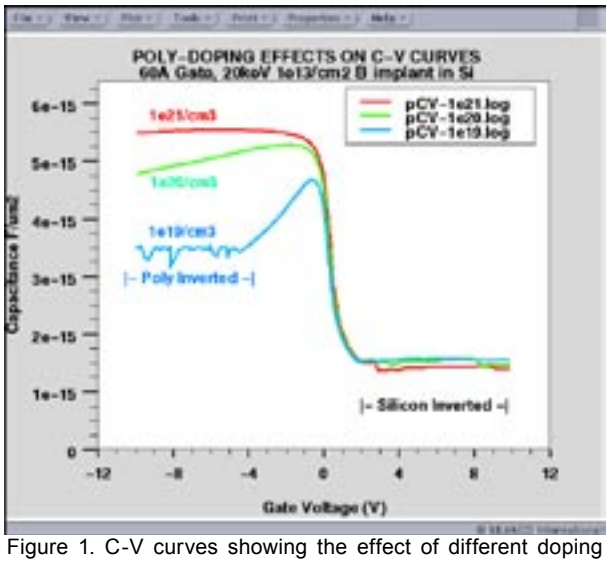

Figure 1. C-V curves showing the effect of different doping concentrations in the poly gate.

Figure 1 shows the results of a simulation using p+ poly of various doping concentrations and a typical channel implant energy/dose of 20keV and 1e13/cm^2 respectively. The silicon substrate was doped 1e15/cm^3 p-type. The oxide was grown in wet O2 at 850C for three minutes resulting in a thickness of approximately 60Å (a typical value for 0.5μm technology). The three C-V plots in figure 1 were calculated in ***ATLAS*** simply by adding the parameters `ac freq=1e6` to the `solve` statement which stipulated 0.2 volt steps from -10 to +10 volts.

Two further parameters were added to the `solve` statement for increased robustness in this case. These parameters were `direct` and `previous`. `Direct` is generally recommended for solving C-V curves whilst `previous` was added to use the previous simulation result as the initial guess for the next step in voltage. This overrides the default initial guess in **ATLAS** which makes a projection from the previous two points. This can cause convergence problems when the solution becomes noisy as in the inversion region.

The reason the solution can become noisy in inversion regions for 1D C-V solutions is that there is no source of the required excess minority carriers as would be the case in a 2D MOSFET device for example. The excess electrons in this case therefore have to be thermally generated in the simulator as they are in reality. It is the requirement of the simulator to accurately account for the total number of these thermally generated minority carriers that is the source of the noise.

Returning to Figure 1, it can be seen that even for a poly doping of 1e20/cm^3, significant depletion occurs in the poly when the channel is accumulated. If a typical automated oxide thickness extract program used the maximum capacitance as the accumulated capacitance and calculated the oxide thickness from this value, it is clear a significant error would result. If the poly doping is reduced to 1e19/cm^3. the poly itself goes into inversion, with a very large effect on the C-V curve and resulting MOSFET I-V curves. When the poly inverts, the noise returns in the calculated curve for the reasons discussed above.

Figure 2 proves that the poly has indeed inverted and shows a close up of the interface regions for a gate bias of -5 volts. Notice how the electron concentration in the P+ poly equals the hole concentration in the bulk of the poly (the usual definition for the onset of heavy inversion).

Figure 2 also demonstrates a very important point when simulating I-V curves in MOSFETs in general. Note the dimensions of the inversion and accumulated regions. The ***entire*** depletion region in the poly is significantly less than 100Å wide. The actual inverted region in a MOSFET channel (responsible for the drive current) is only approximately 10-30Å wide. It is therefore VERY important when accurately simulating I-V curves in MOSFETs that the mesh size in this region is ***no larger*** than 10Å per mesh point. If the inversion region is 30Å wide, a 10Å grid will still only provide 3 grid points in this sensitive region. In this example, the carrier concentration changes from 300 to 1x10^{19} in less than 100Å at the poly-oxide interface.

Conclusion

For sub-micron simulations where polysilicon depletion is likely:

(1) Do not define the polysilicon gate region as the contact. Use an additional metal layer.

(2) In order to obtain accurate device simulation results, ensure that *all* relevant process steps are included and that the process steps are both realistic and accurate. Be especially careful to include any native oxide on the poly during thermal activation.

(3) Use a 10Å grid or smaller at the semiconductor-oxide, poly-oxide interfaces.

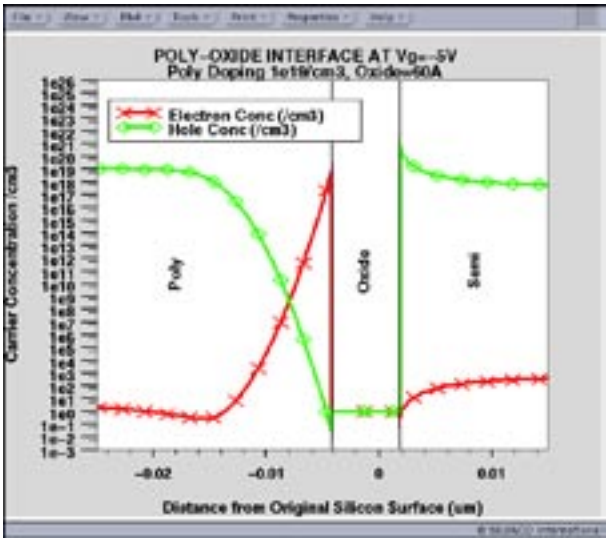

Figure 2. Carrier concentrations at the Oxide-Polysilicon interface showing inversion in the polysilicon gate.

Mesh Control in ATHENA

Avoiding Problems and What to do If they Occur

Introduction

Mesh control in process simulators is one of the major issues tackled by any user. Over the years the meshing algorithms with ***SSuprem4*** and ***ATHENA*** have been improved to the stage where most arbitrary structures can be solved. New approaches such as automated ***ADAPTIVEMESH*** algorithms or standalone programs such as **DevEdit** exist to help users. However there is often no substitute for a firm grasp of the basic methods of mesh control within ***ATHENA*****.** This article discusses six basic principles that can be used to both avoid meshing problems, and correct problems when they occur. These principles are also relevant for ***ATLAS*****.**

Sometimes a small change in a previously working ***ATHENA*** input file can suddenly have a mesh-related error, and cause the simulation to fail. Typically, ***ATHENA*** will state that it failed an internal self-test check and it recommends that you change the mesh. The small change probably did not cause the mesh error, rather, problems with the mesh existed beforehand, but were not serious enough to cause ***ATHENA*** to fail.

1. Avoid Discontinuities of Mesh Size

Initial Mesh Formation

Having large triangles next to small triangles can cause rounding problems and interpolation problems during the calculation. Transition of mesh size should be gradual.

The mesh syntax in ***ATHENA*** lends itself towards a gradual change in mesh size when constructing the initial mesh in the silicon. For example,the commands below would have a relatively course x mesh on the left side at x=0 of about 0.1 micron, gradually decreasing in size to 0.005 microns at x=0.3, and a constant 0.005 micron mesh spacing to x=0.4, and gradually less dense on the right side of the structure at x=0.6. The y mesh becomes gradually less dense with increasing depth.

```
# ATHENA syntax
line x loc=0.0 spac=0.1
line x loc=0.3 spac=0.005
line x loc=0.4 spac=0.005
line x loc=0.6 spac=0.01
#
line y loc=0.0 spac=0.002
line y loc=0.5 spac=0.05
line y loc=0.8 spac=0.15
```

For reference, a similar syntax using locations and spacing can also be used in **ATLAS.** However, the older mesh syntax in **ATLAS** had neither the simplicity or flexibility of mesh construction and tuning.

```
# old ATLAS syntax, taken from bjtex09.in
mesh         nx=31 ny=31
x.m         n=1    l=0.0    r=1.0
x.m         n=31   l=3.0    r=1.0
y.m         n=1    l=0.0    r=1.0
y.m         n=7    l=0.15   r=1.0
y.m         n=20   l=0.5    r=1.0
y.m         n=31   l=1.5    r=1.0
```

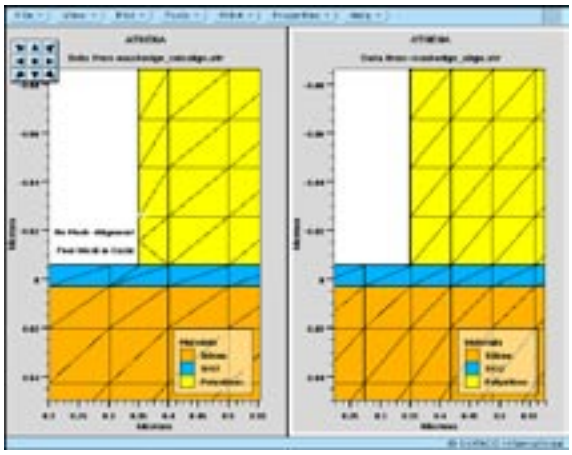

Figure 1. Effects on the Mesh due to Mask Edge. Left - misalignment of poly mask edge and mesh creates awkward mesh in oxide and poly. Right - minor adjustment of mesh aligns mask edge with substrate mesh.

This older ***ATLAS*** syntax is prone to create discontinuities in the mesh size. In this example, for instance, at y=0.5, the mesh size above is 0.026, and below 0.5 the mesh size is 0.09.

Epitaxy, Growth and Deposit

Often, the problem is with the mesh in grown oxide or a deposited material. The x mesh remains continuous into the layers above silicon, but the `y.mesh` is arbitrary.

For deposits, thoughtful use of the `DIVISIONS` option in the `DEPOSIT` statement will prevent discontinuous mesh size.

The mesh in epitaxial layers uses the same syntax as the `DEPOSIT` statement. Users should consider the existing y.mesh in the substrate before deciding upon a mesh in the `EPITAXY`.

For grown oxides, use `METHOD GRID.OX=` <value> to control the thickness of the mesh in the oxide layer. The `METHOD` statement must precede the oxidation step (`DIFFUSE`) for the mesh to be affected. The default value of `GRID.OX` is 0.1 microns, which is too large for some applications. The y.mesh in grown oxides will then have a maximum thickness of this value. Once the value for `GRID.OX` is assigned, it will determine the mesh in all oxidation steps until re-assigned.

2. Include an `x.mesh` Statement at a Mask Edge

In very early versions of ***SSuprem4*** it was almost compulsory for the user to define an `x.mesh` statement at every mask edge. Improvements in ***ATHENA*** have

relaxed this requirement but it is still recommended. This procedure inserts a mesh point at the mask edge, which avoids obtuse and irregularly shaped triangles. Such triangles can cause convergence problems in both ***ATHENA*** and ***ATLAS***.

In Figure 1 the left plot shows an x.mesh at every 0.10 microns, but the poly has been etched at x=0.35. The resulting mesh in both the oxide and poly is less than ideal.

A small change of the mesh statements in ***ATHENA*** can easily rectify the problem. The right plot shows the same region after an `x.mesh` statement at the location of the poly etch.

3. Avoid Thin Triangles

The ratio of the shortest and longest edge of any mesh triangle should ideally be on the order of 10, but not 100. For example, in the meshing program ***DevEdit***, the user has explicit control on this ratio (the "maximum triangle ratio"). Note that in ***TonyPlot***, the default display setting scales the X and Y distances to the window. In this mode, the X andY scale are independent, hence mesh triangle ratios cannot be easily visually determined. To change this setting, Properties... Plot Options...X/Y plot ratio: To data, which will scale the X and Y axes with the same scale.

4. Use Several Mesh Layers in a Material Layer

As a general principle, use more than one mesh layer in a material layer. Users often neglect this principle when forming thin oxides. Even very thin material layers might require three or four mesh layers, despite the potential conflicts with principles 1 and 3 above. A single mesh layer in a grown oxide layer, for example, is inadequate to calculate diffusion of dopants and segregation may also be inaccurate. Partial etching of the material layer will force the mesh to conform to new material boundaries, hence a finer mesh can better accommodate such changes.

This principle is also valid for ***ATLAS*** materials and regions.

There is one minor exception to this rule. The idealized BARRIER layer, through which no implanted ion can penetrate, and does not diffuse any dopant. Gridding in this material can be arbitrary.

5. Avoid Cases of Several Mesh Triangles with a Common Vertex

In a rectangular base mesh, each vertex is shared by six mesh triangles. In some situations, such as corners, edges, and regions of discontinuous mesh size, the mesh may become deformed and have many triangles intersecting at a single point.

Figure 2 shows a case that, due to discontinuous mesh size between materials, and having a single mesh layer in the top material, the mesh has become deformed in this manner.This situation can lead to problems with subsequent process steps in ***ATHENA***.

6. 1000 - 3000 Mesh Points is Adequate For Most Simulations

For a fixed set of models, the simulation time is approximately proportional to the number of points to a power ~ 2.5. Doubling the number of mesh points would generally mean more than a factor of four increase of simulation time.

Increasing the number of mesh points will increase simulation run times, but does not guarantee more accurate results. Obviously too coarse a mesh will definitely lead to inaccurate results. The objective is to place the mesh points in the most strategic locations - material boundaries, implant ranges, diffusion ranges and pn junctions.

Sometimes it is necessary to have a fine x.mesh near or at the surface, but due to the mesh construction, an undesirably large number of x.mesh points will be present in the lower part of the structure. The `RELAX` statement is a useful command to reduce the mesh density in substrate areas. The grid can be relaxed independently in the x and y directions. For example:

```
RELAX  x.min=0.0  x.max=1.0  y.min=3  y.max=6
dir.x=true dir.y=false
```

will the x.mesh density, but not the y.mesh, and only in the specified location. Note that `RELAX` works only with rectangular base grids and will not eliminate grid lines next to a material boundary. Typically, each second mesh line is removed.

Conclusion

These principles will correct most mesh-related problems in ***ATHENA***. Increasing the density of the mesh will not fix all problems. Sometimes, decreasing mesh density, or more often, changing the location of the fine mesh area will correct the "internal self check failed" mesh related error.

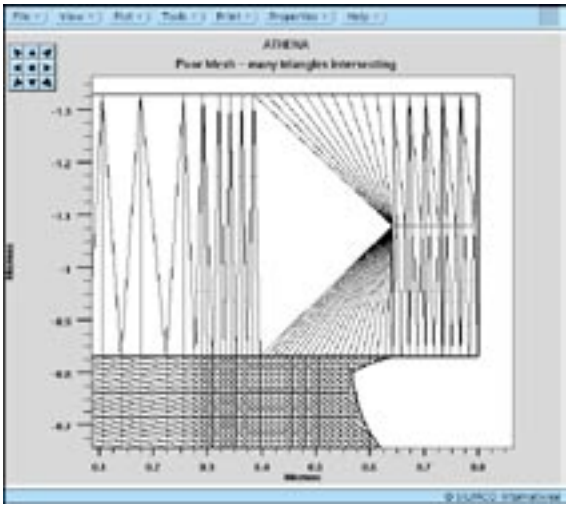

Figure 2. Mesh triangles sharing a common vertex. Due to discontinuous size mesh between materials, the mesh in the top layer is distorted.

Calendar of Events

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March

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31 W/S - Grenoble, France

Bulletin Board

Parallel ATLAS on HP Servers!

Silvaco announces the availability of Parallel ATLAS on HP 9000 Exemplar technical servers, running HPUX 11.0. This includes K/V/X-Class servers. Parallel ATLAS speeds up a simulation job by exploiting the multiple CPU architecture of these servers. This comes in addition to the previously available Parallel ATLAS on Sun Enterprise and Ultra servers running Solaris 2.4-2.6 as well as SGI powerchallenge and Origin servers running Irix 6.2 and 6.4.

See Silvaco at San Francisco DAC!

Silvaco will be exhibiting the latest in TCAD Driven CAD tools at the Design Automation Conference. The exhibition will be 15-17th June at the Moscone Center, San Francisco. Silvaco will present the latest advances in:

- SmartSpice
- NT-based Layout and Verification Tools
- Technology based Parasitic Extraction
- 3D TCAD

New Manager for Boston Office!

Michael Ridinger has joined Silvaco in the capacity of applications manager for the North Eastern region. He brings many years of hands-on experience from Allegro Microsystems. His charter is to aggressively build up a team of applications engineers to better serve customers in this region.

If you would like more information or to register for one of our our workshops, please check our web site at ***http://www.silvaco.com***

Hints, Tips and Solutions

William French, Applications and Support Manager

Q: How can external tools be run inside of Silvaco's run-time environment *DeckBuild*? Is it possible to include UNIX commands along with simulator syntax inside an input file?

A: The run-time environment for all Silvaco TCAD simulators, ***DeckBuild***, allows users to include any UNIX command inside any simulator input file. The option uses the keyword `SYSTEM` before the UNIX command. Some users might find this option may need to be enabled using the OPTIONS category from the MAIN_CONTROL popup menu.

Any UNIX command or sequence of commands linked by ';' can be executed when preceded by the `SYSTEM` keyword. For example to remove a set of files before creating a diffusion movie:

```
system rm xxx*
diffuse ..... dump=1 dump.pref=xxx
```

The only major exception to standard UNIX syntax is the use of the output redirect command '>' in UNIX. This cannot be used by `SYSTEM` since the output of the UNIX command will be redirected to the lower or run-time output window in **DeckBuild**. The following syntax can be used instead to output an extracted variable to a file.

```
#extract threshold voltage
extract name="vth" \
xintercept (maxslope(curve(v."gate",i."drain")))
\
- ave(v."drain")/2.0

# save Vth to a file called
xxx.dat system echo $vth | sed -n "w xxx.dat"
```

The inclusion of any valid UNIX command within a simulator input file allows users to include their own simulators or other external routines inside **DeckBuild.** For example to call a program 'myprog' that reads and writes Silvaco format files might be called using:

```
# save ATHENA structure
structure outf=final.str
# run external program to create a new structure
system myprog final.str revised.str
#load new structure into ATHENA
init inf=revised.str
```

Q: Is it possible to model leakage current due to localized trap centers in the vicinity of depletion regions?

A: ***ATLAS*** version 4.3.0 includes a trap assisted tunneling model [1] that accounts for band-band tunneling assisted by traps. The model accounts for trap location, density and energies defined using the `TRAP`, `DEFECT` or `DOPING` statements. This model supercedes the `TATUN` model implemented in earlier ***ATLAS*** versions. To enable the model the syntax is:

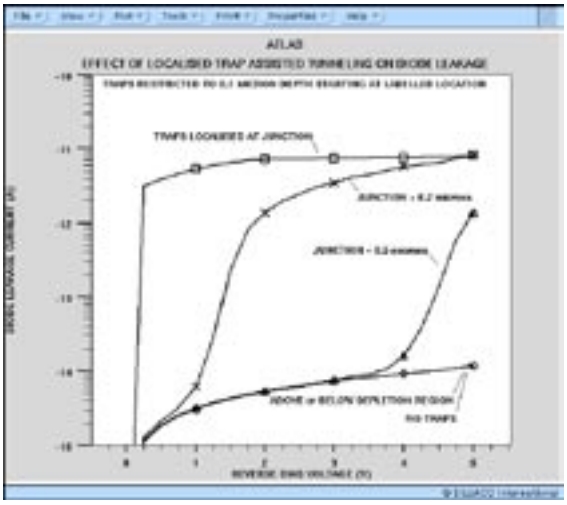

Figure 1. **ATLAS** simulation of leakage current based on traps located close to a pn junction.

MODEL TRAP.TUNNEL

With this model it is possible to simulate the effect of localized trap densities. Most commonly the effect of localized traps is seen when they are within the depletion region of a reverse biased diode, including in the drain junction area of MOSFETs. Figure 1 shows the reverse leakage current of a source/drain diode as a function of the location of trap centers. When the traps are wholly inside the source/drain region or deep enough in the substrate to be outside the depletion region the results are identical with the case including no traps at all. However when the traps are localized in the junction region the leakage current is 3 orders of magnitude higher. Traps located just deeper than the junction only have an effect when the depletion region extends deep enough to reach them as shown by the intermediate curves in Figure 1. Localized trap centers in devices might be caused by plasma etch damage, contamination or extended defects.

[1] Hurkx, G.A.M., Klaassen, D.B.M, and Knuvers, M.P.G. "A New Recombination Model for Device Simulation Including Tunneling", ED. 39, No. 2, Feb. 1992, pp. 331-338.

Call for Questions

If you have hints, tips, solutions or questions to contribute, please contact our Applications and Support Department

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e-mail: support@silvaco.com

Hints, Tips and Solutions Archive

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