CLEVER - Process Technology Based Extraction and Optimization of Custom Cell Parasitics

Introduction

Silvaco has recently released a new suite of interconnect analysis tools to meet the demands of state of the art cell, circuit and chip design. Next generation IC's are now being designed with sub-0.25μm CMOS technology and submicron multi-level interconnect systems. It is becoming increasingly clear that this combination of advanced technologies requires accurate values for the parasitic R and C components. Without such considerations CAD engineers will face an almost impossible engineering task both today and in the near future.

Traditionally these parasitic components have been calculated based upon empirical models or at best two-dimensional device simulations. Both of these methods are now exhibiting questionable values as 3D fringing effects become severe and 3D layouts become more common. CLEVER has, at its fundamental core, an advanced fully 3D backend process simulator ODIN which is able to finally provide the solution CAD engineers have been waiting for.

Figure 1. Accurate parasitic extraction for an exclusive NOR cell requires realistic interconnect geometries.

This article will illustrate the application of CLEVER beginning from layout information, through 3D process simulation and finally extraction of the parasitics. As the subject for this study an exclusive NOR cell (EXNOR) design has been chosen. CLEVER will be required to produce a netlist of the parasitic capacitance, resistance and active devices. This netlist is automatically back annotated and therefore immediately available for analog circuit simulation.

A Layout-Driven Approach

The CLEVER design phase is centered around an easy to use GUI designed to allow efficient data handling and seamless integration of the individual tasks required for extraction (Figure 3).
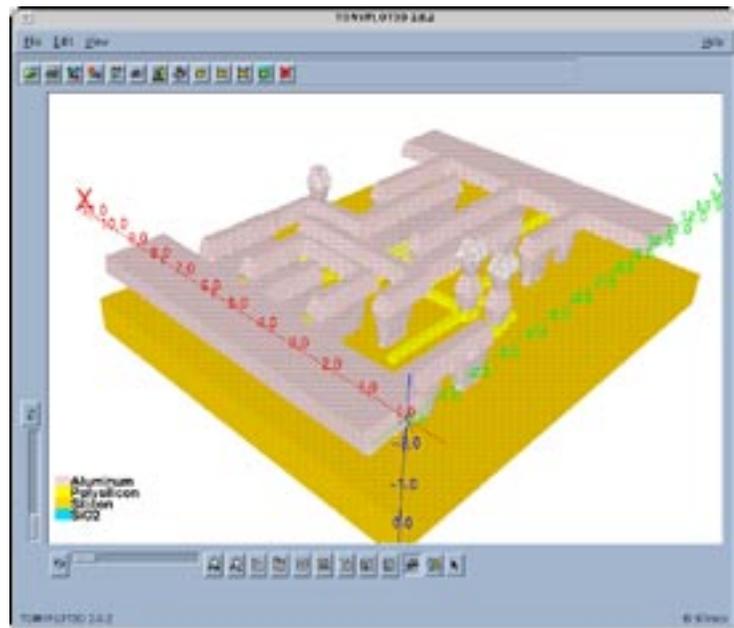
The starting point for CLEVER analyses is to import a GDSII file into the MASKVIEWS layout editor where the designer may save the entire cell or choose a portion of the cell for the analysis. In this application the entire EXNOR cell in Figure 2 will be analyzed.
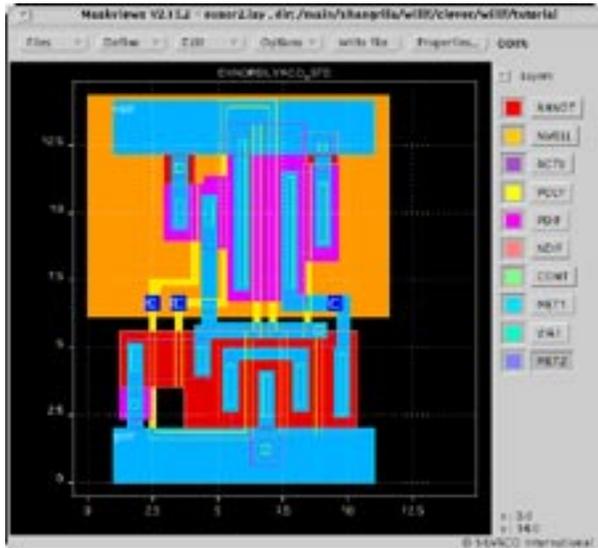
INSIDE

Figure 2. Original GDS-II layout of exclusive NOR cell. Node labels are read from GDS-II file.

Figure 3. A file manager stores and organizes inputs and results from CLEVER.

3D Process Simulation

In any advanced custom cell, such as in Figure 2, there will be many areas of prime importance. These could include linewidth variations, corner rounding, non-uniform etch rates and lithographic effects. Four major types of structure which CLEVER can handle are

(a) manhattan structures where etching results in ideal rectangular block shapes

(b) non-manhattan structures that exhibit the effects of isotropic etching

(c) lithographic effects where etching depends on the photoresist exposure

(d) multi-metal interconnects with multiple dielectrics

CLEVER uses the 3D process simulator ODIN designed to allow all these variables to be taken into account inside a single custom cell. This was achieved by linking layout information generated from MASKVIEWS to the process information required by ODIN. For the purposes of this article the EXNOR design has been performed for a non-manhattan structure as shown in Figure 1.

An additional underlying rule was that the 3D tool should remain usable for engineers with little TCAD experience. Therefore the amount of information required in the process input deck has been made as minimal as possible. This has been helped by the development of a proprietary 3D tetrahedral based, adaptive meshing algorithm that results in virtually no user intervention. A benefit from this is that the number of mesh points required is minimal as can be seen by the mesh shown in Figure 4.

The 3D process simulation capabilities are technology independent and support multiple dielectrics, arbitrary metals and polysilicon.

3D Parasitic Extraction

The field solver within CLEVER allows the calculation of the resistance and capacitance. In order to do this information must be provided to identify the active devices in the cell. This is accomplished with the aid of a technology file that applies Boolean logic to the mask layers in order to identify the active areas.
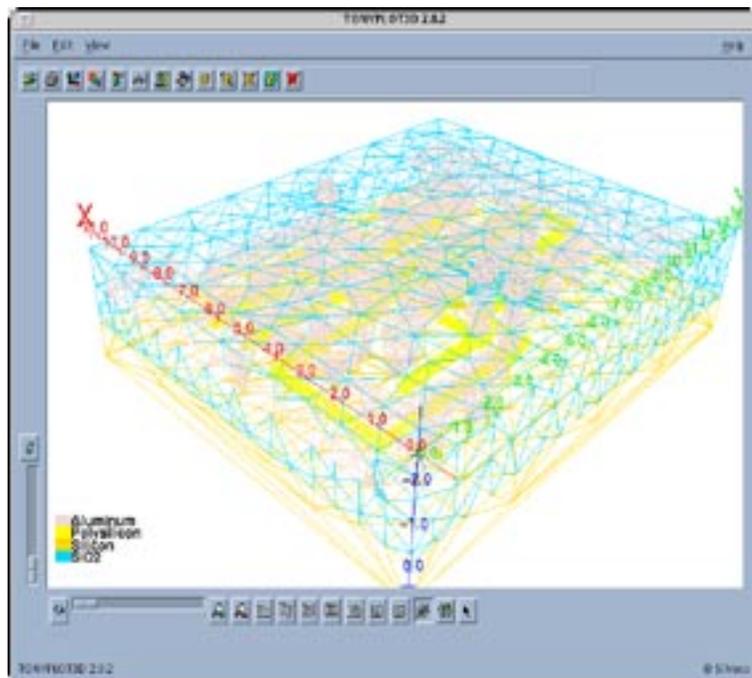

Figure 4. The 3D adaptive meshing in CLEVER requires no user intervention beyond specifying the desired accuracy of the final parasitics.
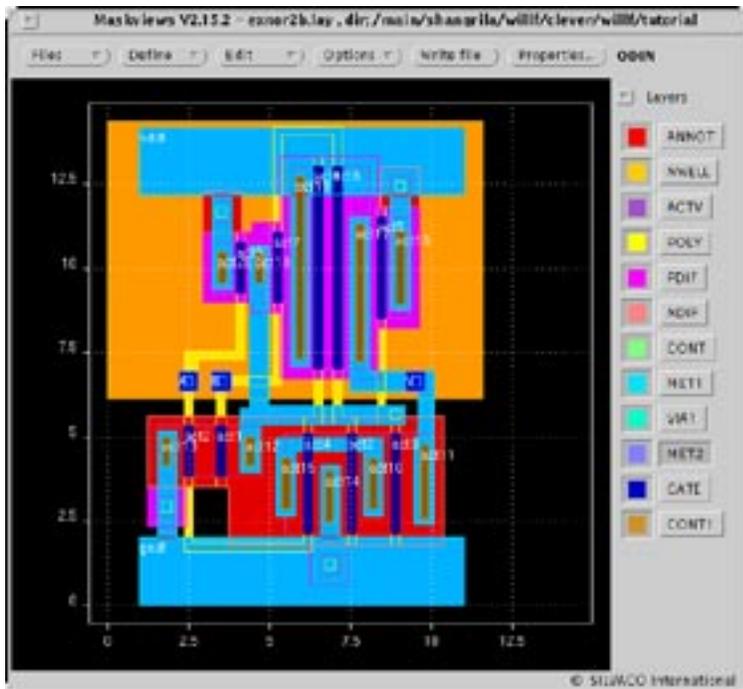
Figure 5. EXNOR layout annotated with internal node locations. The internal nodes are used for back-annotation to the netlist.

CLEVER extracts the active device connectivity. Active devices are saved to the netlist with width, length and other geometrical SPICE parameters. This will allow the correct junction capacitance in future SPICE simulations to be included automatically. Once identified they are removed from the electrical analysis. CLEVER will also introduce extra contact nodes into the layout in order to "split up" complicated metal paths so that a distributed RC spice netlist is obtained. These extra, or auxiliary, nodes are then back annotated onto the layout and can be viewed using MASKVIEWS. Figure 5 shows the new layout file obtained for the EXNOR under analysis.
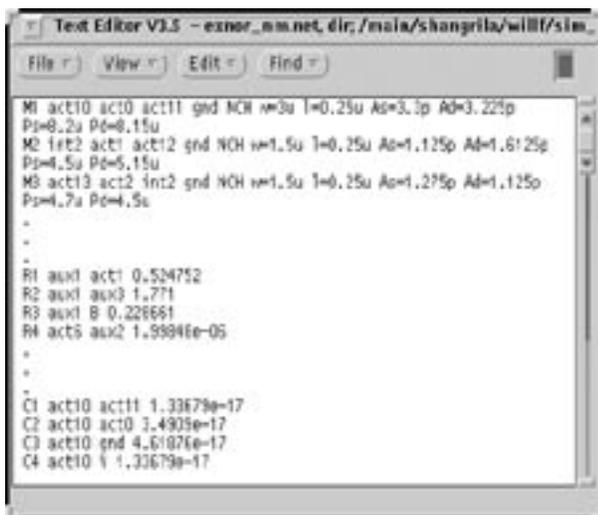

Figure 6. Netlist produced by CLEVER includes active devices as well as parasitics. Back-annotation with original node labels is available.

The extracted parasitics are annotated into a netlist according to the node names in the GDSII file, although custom node names can be added using MASKVIEWS. A portion of the netlist generated for the EXNOR is shown in Figure 6.

SmartSpice Circuit Analysis

To illustrate the circuit performance obtained from CLEVER analysis three examples are studied - the EXNOR cell, an inverter cell and a buffer circuit. These will illustrate some typical uses of CLEVER.

The netlist produced from the CLEVER analysis of the EXNOR cell can be used to illustrate the dependence of interconnect and junction capacitance effects on the delay times, as shown in Figure 7. Using CLEVER engineers can optimize design parameters and immediately know the influence on circuit performance.

To take a simpler example, Figure 8 shows the layout of an inverter cell designed with NMOS and PMOS transistors. CLEVER has been used to analyze this cell under three processing conditions - manhattan, non-mahattan and lithographic etching. The extracted netlists have been used within a 9 stage ring oscillator circuit in order to show the effect on circuit per-
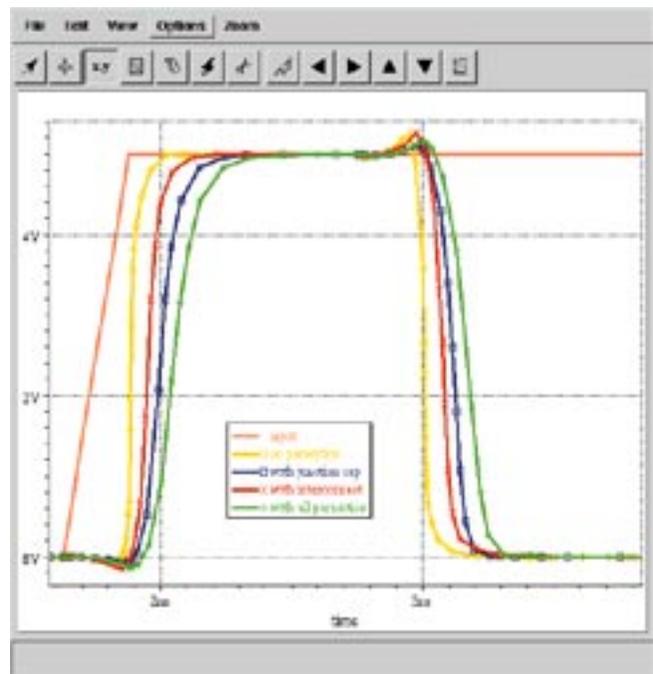

Figure 7. SPICE simulation showing the effect of interconnect parasitics on timing of the EXNOR cell.
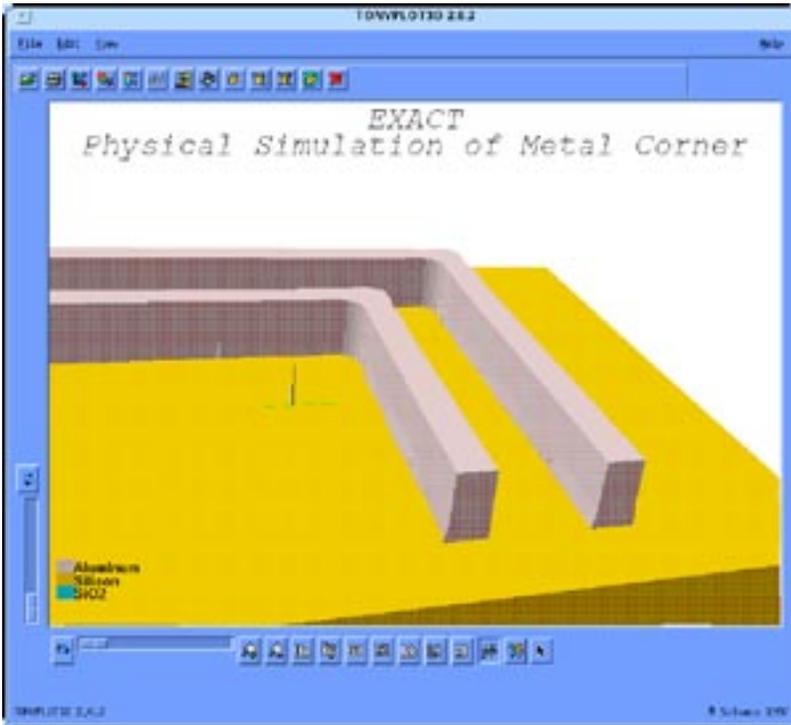
Figure 8. CMOS inverter layout used to compare different inter-
connect geometry models.

Figure 11. Effects of different metal widths on inverter's gate
delay are plotted.

formance. Figure 9 shows the influence of the processing conditions on the delay times and clearly illustrates the importance of obtaining accurate information on the parasitic components.

Finally, the effect of varying metal linewidths has been examined based upon the buffer circuit layout in Figure 10. Within the SmartSpice deck an inverter load has also been implemented. Figure 11 shows the effect of different metal linewidths, for the metal 2 layer, on the resultant delay times for this circuit.

Multi-Metal, Multi-Dielectric Structures

CLEVER can handle interconnect structures of arbitrary complexity. In modern processes a description of purely aluminum interconnects embedded in a homogeneous

oxide dielectric is wholly inaccurate. The use of Tungsten plugs, anti-reflective coatings, low k dielectrics and copper interconnects are increasingly common. Extraction of resistance becomes a non-trivial problem in this case. Figure 13 shows an SRAM cell simulated with multiple metal materials. Since the metal interconnects are coated with liner and barrier layers, Figure 12 shows a 2D cross section of this structure for greater clarity. In addition to the multiple metal materials this cell also has 45 degree layout. The traditional 'counting squares' methods are insufficient for half-micron technology. Conductivities and permittivities of arbitrary materials are easily defined in the syntax of CLEVER. The netlist produced from this cell reflects the resistive effects of copper and tungsten.

Figure 9. Effect of using idealized geometries vs. realistic inter-
connect process simulation on ring oscillator gate delay.

Figure 10. Metal sepentine used to examine metal width effects.

Figure 12. 2D cross-section of SRAM cell showing multiple metal materials.

Figure 13. SRAM cell with 4 metal layers plus polysilicon. Each metal layer is composed of multiple material layers which are correctly modeled by CLEVER for accurate resistance extraction.

Conclusion

Technology has reached the stage where engineers now require much more accurate information on the parasitic components within custom cells and their effects upon circuit performance. This can now only be achieved through the use of a fully 3D process simulator with an easy to use user interface. This article has shown some of the basic operation of CLEVER and the types of analysis engineers will be capable of performing.

EXACT - Process Technology Based Interconnect Parasitic Library Generation

EXACT is a new tool that enables engineers to build process dependent behavioral models (RSMs) of interconnect parasitics for a given technology. Results from EXACT are used by IC design LPE tools in the extraction of full chip interconnect parasitics. EXACT is based on a combination of advanced 3D TCAD process simulation, an accurate 3D electrical field solver, and innovative Design Of Experiment (DOE) automated structure generation and curve fitting utilities.

EXACT is tightly coupled with the lithography, deposition and etching modules of Silvaco's advanced 3D backend process simulator ODIN. Users can define arbitrary multi-layer parameterized test structures using the interactive or DOE capabilities within EXACT , and simulate the true process-dependent 3D geometry of the structure. The parasitics for the structure are calculated using an accurate 3D field solver that account for effects such as multiple dielectrics and shielding. The resulting para-

sitic values calculated using EXACT supplement existing LPE environments by providing highly accurate parasitic models and technology rules that describe the impact of process-related variations and design changes on the properties of the interconnect structures.

Process Dependence of Interconnect Extraction

With the drive to sub-half micron technology, the complexity of interconnect geometry extracted using a realistic process simulation have more and more influence on the electrical models of the interconnect as the clock frequency increases. There is no doubt, that only 3D field solver calculation of the interconnect parasitics should be strongly linked to process simulation. This means that the 3D field solver must be applied to interconnect geometries obtained from the correct process flow as opposed

Figure1: Metal Elbow structure using realistic etch and lithography models. Effects on metal profile and corner rounding are clearly seen. The resulting capacitance is over 25% different from a simple 'rectangular block' approximation to the geometry.

Metal Geometry	Capacitance
IDEALIZED	0.60fF
with ETCH	0.57fF
with LITHOGRAPHY	0.47fF
with ETCH+LITHOGRAPHY	0.44fF

Table 1. Comparison of inter-metal capacitance for the Metal Elbow structure in Figure 1.

to solid modeling approaches used by other parasitic extraction tools. The irregularities will become more important as the frequency increases. An example of the large effect on capacitance for a simple metal elbow structure is given in Table 1. Over 25% difference in capacitance is seen between the realistic structure and a simple 'rectangular block' approximation (Manhattan geometry).

Who needs results from EXACT?

Verification Engineers: EXACT provides LPE tools with accurate models to be used to extract the interconnect parasitics of a chip. These models are built taking into account not only the "geometrical" process parameters (dielectric and metal thicknesses, dielectric permittivity) but also the "physical" process parameters (lithography, deposition and etching models).

Designers: EXACT is a powerful tool to calculate accurately the interconnect parasitics (not just capacitance) as functions of design parameters (Metal Width, Metal Space). This parasitic information is needed for accurate analog circuit simulation for such design targets as timing, power analysis, signal integrity.

Process Engineers: Characterized models from EXACT show the effect of process changes on test structure measurements. Process effects such as dielectric thicknesses, multiple metal layers and lithography can easily be analyzed.

Easy to Use GUI

The goal of using EXACT is to build behavioral models for interconnect parasitics as a function of process and layout variations. This approach to simulation is used successfully in the 'Virtual Wafer Fab' for TCAD applications. The EXACT user interface simplifies the task of definition of input process flow, parameterized layouts and experimental designs. The GUI also acts as a data manager to store results as worksheets, equation fits and as RSM models. It also allows export of the final interconnect libraries to LPE tools.
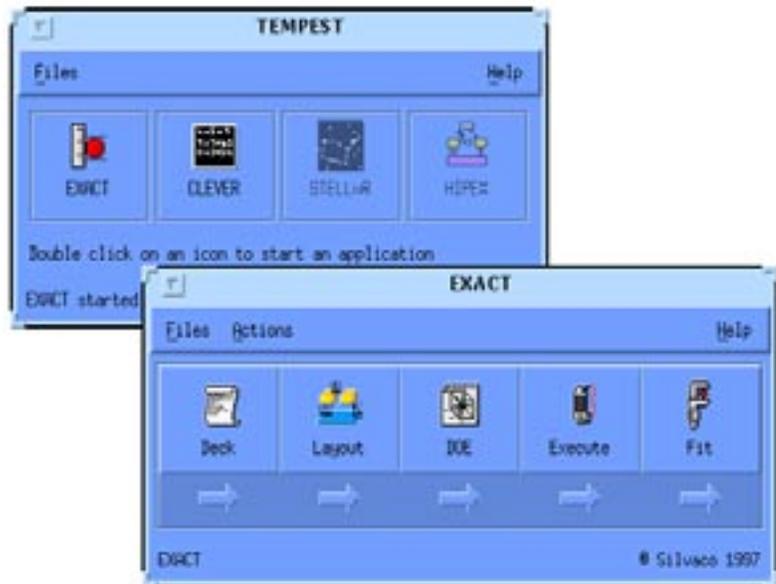
Figure 2: The Graphical User Interface for EXACT guides users in the creation of fitted technology dependent interconnect models.
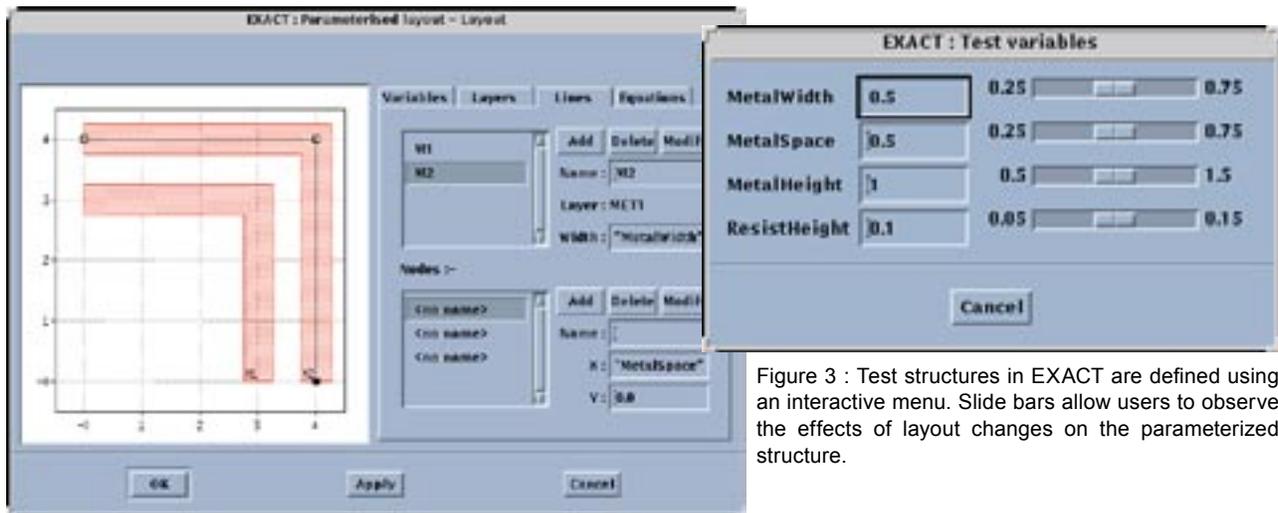
Figure 3 : Test structures in EXACT are defined using an interactive menu. Slide bars allow users to observe the effects of layout changes on the parameterized structure.

Interactive Test Structure Definition

To extract interconnect parasitics as a function of geometry, it is necessary to define parameterized interconnect test structures. EXACT features an interactive GUI for arbitrary structure definition. Test structures are defined as 'sticks'. Easy-to-use slide bar controls on variables such as metal width or space allow users to prototype the process variations (Figure 3). EXACT also supports text-driven batchmode layout commands for advanced users.

Experimental Design

Design of experiments (DOE) is a key feature of EXACT. When the number of process and geometry variables becomes high the number of separate simulation runs can escalate. DOE is used to optimize the number of simulation runs actually required to generate a behavioral model (Figure 4).
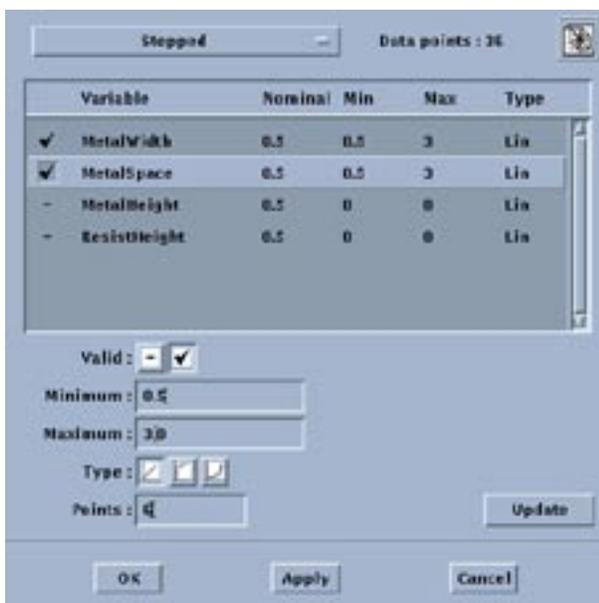
Figure 4: Design of Experiments setup menu for EXACT. DOE setups may be saved and loaded from the EXACT data manager.

Analyzing Behavioral Models for Interconnects

The resistance and capacitance extracted from each structure are archived in worksheets with the related design and process data. EXACT provides built-in features for the creation of technology rules that represent the parasitic values as a function of design and/or process parameters.

A data fitting utility creates arbitrary equations to be used in LPE tools that describe the relationship between the parasitic values and the underlying process and design parameters of the structure. Visualization capabilities are available to view the resulting 2D and 3D behavioral models.

Calibration to Silicon

The accuracy of interconnect parasitics is crucial to the success of modern deep sub-micron designs. Parasitic extraction tools must be able to provide dependable resistance and capacitance values over the full range of
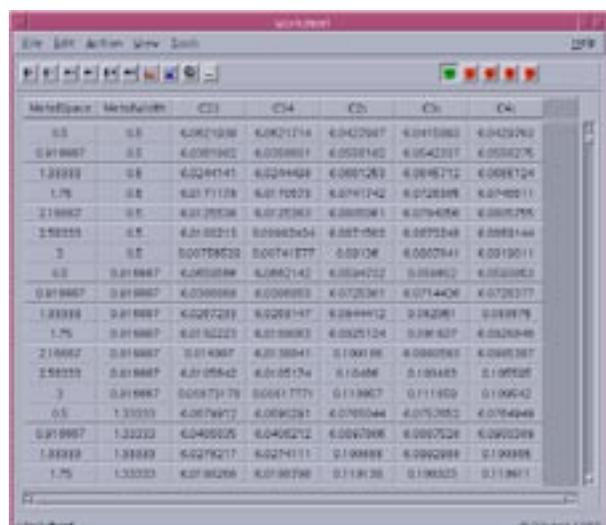
Figure 5 : Worksheet of raw capacitance vs. geometry data.

Figure 6 :EXACT fits pre-defined or user generated equations to the raw data.Coefficients in the equations are optimized to provide the best fit

Figure 7. Behavioral model of inter metal capacitance as a function of metal width and space.

manufacturing variations. The capabilities of EXACT have been developed to meet this criterion. The behavioral models that are generated describing resistances and capacitances as functions of geometric design and physical process param-

eters can be compared to measured capacitance data for calibration. Isolated experiments can be used to optimize design parameters for a given process, or to optimize critical process parameters to meet circuit performance requirements.

Blaze Simulation of SiGe:Si Heterostructure p-MOSFETs

P. A. Clifton, and A. G. O'Neill*
*Department of Electrical and Electronic Engineering, University of Newcastle, UK.

Introduction

The 2-D heterostructure device simulator Blaze is used here to investigate the design criteria for sub-micron p-channel SiGe:Si heterostructure MOSFETs. Thin layers of compressively strained SiGe grown 'pseudomorphically' on silicon substrates exhibit improved in-plane hole drift mobility relative to Si (800 cm^2/V.s [1] c.f. 450 cm^2/V.s) and may be applied in future enhanced p-channel devices (as shown schematically in Figure 1) for high performance CMOS. The use of a buried channel is also expected to improve carrier mobility and noise performance by reducing the interaction of carriers with the oxide interface. A major constraint on HMOSFET performance is the onset of parasitic inversion at the cap-oxide interface where carriers have degraded mobility. This limits the degree of inversion in the strained channel layer by electrostatic screening and hence degrades the small signal transconductance.

Device Simulation

Numerical simulation based on ATLAS-Blaze is used here to explore the design parameter space for enhancement (inversion) mode SiGe p-HMOSFETs. Fermi-Dirac statistics for carrier populations and a dense mesh
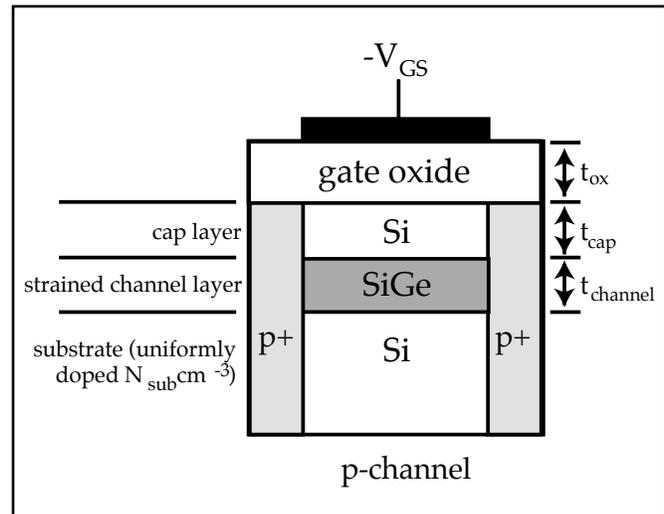
Figure 1. Schematic of the strained SiGe p-channel heterostructure MOSFET.

specification for the thin epitaxial layers are required for accurate modeling of charge distributions and drift-diffusion based current formulations have been found to be sufficient for the range of channel lengths investigated (down to 0.25μm).

The epitaxial cap and channel layers in the simple device structure are assumed to have low background doping (5×10^{13} cm^{-3}) and the underlying substrate (or n-well) uniformly doped to varying degrees (N_{sub} cm^{-3}) in the range 1×10^{16} cm^{-3} to 5×10^{17} cm^{-3}. Interface states are neglected, a p+ polysilicon gate is used and the threshold voltage is allowed to shift freely according to channel doping and layer thicknesses.

D.C. output characteristics and small signal transconductance have been obtained (the latter by AC analysis [2]) and the respective inversion layer carrier populations in the cap and channel have been extracted by integrating the carrier profiles across the total depths of these layers. The region of integration was defined midway between source and drain at zero drain bias so as to avoid the complicating effect of junction depletion regions.

Density of States in Strained Layers

A reduced effective density of states (DOS) in the valence band, N_V, is inherent in the use of compressively strained SiGe channels on Si [3], being intimately linked to the enhanced hole mobility [4,5]. The lower density of states effective hole mass and the reduced carrier scattering due to the lifting of the valence band degeneracy are both thought to contribute to higher μ_h. As the Ge fraction in a strained SiGe layer, x, is increased, N_V is predicted to fall monotonically [5] - by a factor of 5.6 at x=0.3, an effect that should not be ignored in modeling HMOSFETs.

Benchmarking

An experimental 0.7 micron channel length SiGe p-channel MOSFET reported by Nayak et. al. [6] has been used as a benchmark to support the validity of the simulation results. In modeling this device, which had a SiGe composition factor x=0.2, the effective N_V in the SiGe channel layer was reduced from 3.09×10^{19} cm^{-3} to 7.09×10^{18} cm^{-3} according to [5] and the band offset was taken as 0.15eV based on the mean of the reported values collated in [7]. The carrier mobility in the surface channel was assumed to be degraded with increasing transverse and longitudinal fields using the 'CVT' model [8] and the mobility in the SiGe channel was assumed to be insensitive to the transverse field. By using only the layer mobility values as fitting parameters (μ_h =185 cm^2/V.s in the SiGe and μ_h(max)=255 cm^2/V.s in the Si cap), a good fit to the experimental transconductance curves has been obtained, as shown in Figure 2(a). Extracted inversion layer carrier concentrations, shown in figure 2(b), indicate that the level of inversion in the SiGe channel is in fact very low in these devices and that the main contribution to the drain current comes from the undesirable surface inversion layer in the silicon cap.

The effect of a reduced density of states on the carrier concentration in the strained channel is marked, as shown in Figure 2(b), where the saturated carrier concentration falls from 1.19×10^{12} cm^{-2} to 0.83×10^{12} cm^{-2} when N_V in the SiGe is reduced by strain from 3.09×10^{19} cm^{-3} to 7.09×10^{18} cm^{-3}. Neglecting the reduction in N_V is liable to lead to falsely low extracted hole mobilities in experimental devices due to overestimation of carrier concentrations in the SiGe channel.

Response Surface Methodology.

In order to thoroughly explore the large parameter space which determines the performance of a HMOS-FET, the experimental $0.7\mu m$ channel length device [6] has been taken as the basis for an investigation by response surface methodology (RSM), a feature of the VWF Automation Tools. The dependencies of the SiGe: Si valence band offset and the hole mobility on SiGe layer composition (x) were respectively modeled as $\Delta E_V = 0.75x$ eV [11] and $\mu_h(SiGe) = 750x$ cm^2/V.s, a conservative assessment of hole mobility based on early literature values [6] [9] [10] for experimental devices. The drawn channel length was maintained at $0.7\mu m$ and N_V in the SiGe was fitted to the data given in [5].
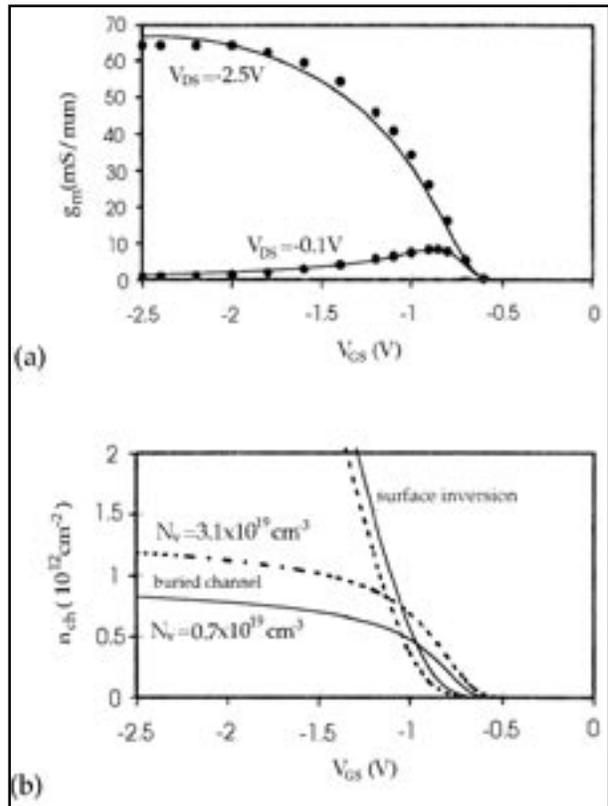

Figure 2.

(a) Transconductance curves obtained by simulation using the fitted model for a $0.7\mu m$ gate length p-HMOSFET. Upper curve is for device in saturation (V_{DS}=-2.5V) and lower curve is linear (V_{DS}=-0.1V). The dots represent the experimental data reported by Nayak et. al. [6].

(b) Surface and channel inversion layer hole concentrations obtained for the same device, both with full (3.09×10^{19} cm^{-3}, dotted lines) and reduced (7.09×10^{18} cm^{-3}, full lines) DOS in the strained SiGe.

The same calibrated device model was used throughout and a 2^4 full factorial design based upon a body centered cubic structure was implemented with the four input factors; oxide thickness (t_{ox}), cap layer thickness (t_{cap}), substrate doping (N_{ox}) and Ge composition in the channel (x). Previous (unreported) studies have shown that neither the channel thickness nor the presence of a spacer layer between the channel and the doped substrate play a significant part in the device performance and hence these factors are neglected here.

Three key output metrics have been modeled as functions of the four input factors: n_{ch}(max) - the maximum hole concentration achieved in the SiGe channel with V_{GS} = -2.5V, ΔV_{GS} - the gate voltage range above the threshold voltage over which the integrated inversion charge in the SiGe exceeds that in the cap and g_m(max) - the maximum transconductance obtained with V_{DS} = -2.5V.

A wide range of functional relationships can be examined between each of the output factors and the four input factors, usually by the use of response surface plots. Selected cuts through the 4-dimensional factor space of the experiment are presented in figures 3 to 5 to illustrate major trends.

Discussion

It may be seen in Figures 3-5 that all the metrics of device performance; n_{ch}(max), g_m(max) and ΔV_{GS} generally deteriorate as the thickness of the cap layer is increased.
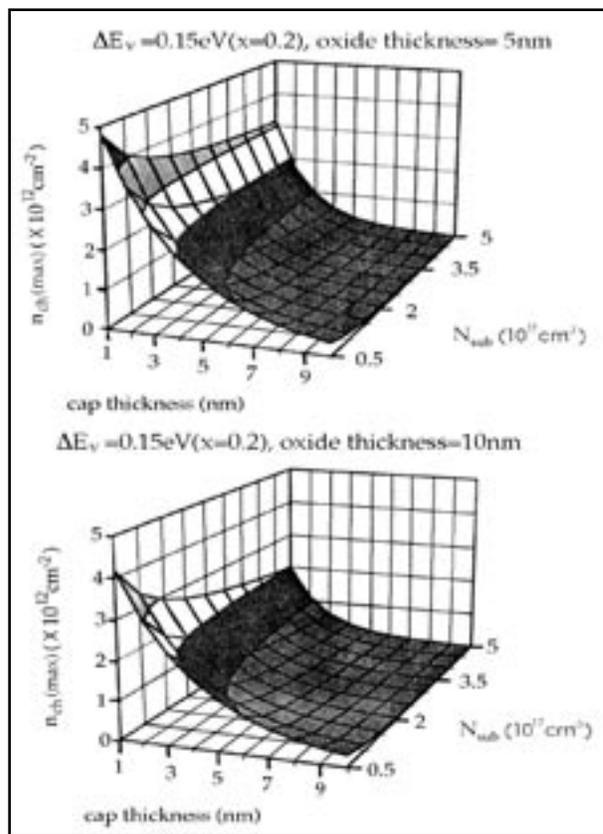
Figure 3. RSM results obtained for the device represented in Figure 2.
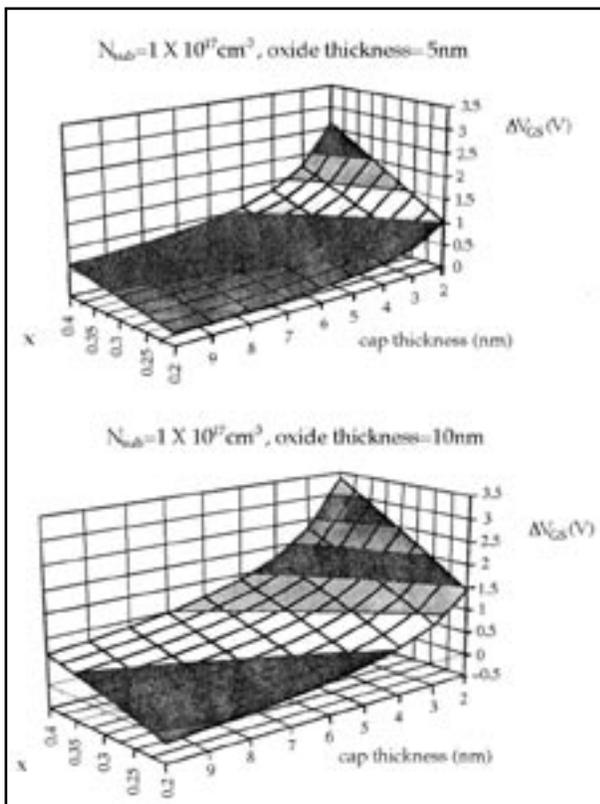
Figure 4. RSM results obtained for the device represented in Figure 2.
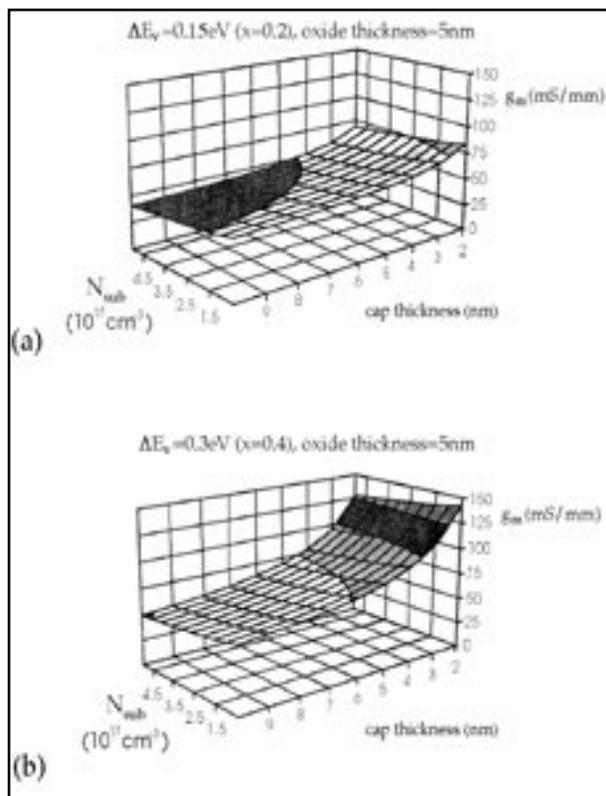
Figure 5. RSM results obtained for the device represented in Figure 2.

This is particularly important at high substrate doping levels (Figure 3) which lead to strong band bending (high transverse field) in the channel region under gate bias. The threshold for parasitic surface inversion is consequently reduced relative to that for SiGe channel inversion, so causing ΔV_{GS} to decrease. A smaller useful range ΔV_{GS} is concomitant with reduced SiGe inversion charge and hence smaller transconductance. In Figure 4, $g_m(max)$ can be seen to fall as t_{cap} and N_{sub} increase. The use of a large value of band offset (high x) improves ΔV_{GS} markedly, as expected (Figure 5), since the threshold voltage for inversion of the buried channel is reduced relative to that of the surface channel. It is important to note that the role of the band offset is not so much in providing carrier confinement in the strained SiGe as in allowing an inversion layer to be induced in the SiGe rather than at the oxide interface. That is, a smaller offset does not degrade performance by allowing carriers to leak out of the SiGe potential well but rather it reduces the critical bias range ΔV_{GS}.

A thinner gate oxide also results in a higher $n_{ch}(max)$ (not shown) and hence improves current drive and $g_m(max)$ due to the improved capacitive coupling between gate and channel charges. These improvements in performance will always overcome the disadvantage of the small reduction in ΔV_{GS} arising with the thinner oxide which is evident in comparing Figures 5(a) and (b).

Deep Sub-micron HMOSFETs.

It has been seen that the main limitations on HMOSFET operation arise at high levels of sub-channel doping, i.e. under the conditions associated with deep sub-micron devices. A great benefit of RSM is that any combination of input factors (within the modeled parameter space) may be inserted into the derived empirical RS model to determine a good estimation of the device performance. For example, taking a typical 0.35µm MOSFET with $N_{sub} = 4.5 \times 10^{17}$ cm^{-3} and a 9nm thick oxide, negligible conduction in the SiGe channel is achieved for $x=0.2$ and the channel population is still rather limited for $x=0.4$ unless very thin cap layers are employed. Going a stage further to a 0.25µm channel length p-HMOSFET with $N_{sub} \cong 5.5 \times 10^{17}$ cm^{-3}, ΔV_{GS} may diminish to zero (the surface inverts before the channel) even for a cap thickness as small as 7nm. This is illustrated by the simulation results shown in Figure 6 ($\delta=0$) for a device based on the one reported by Kesan et. al. [10] ($\Delta E_v=0.15eV$). This device was simulated using the same numerical model as for the Nayak [6] HMOSFET but fitting values of 350 and 300cm^2/V.s for the maximum channel and cap layer mobilities respectively. The graph of integrated sheet hole concentrations, Figure 6(b) ($\delta=0$), shows that this structure supports very little inversion charge in the buried SiGe channel. It is possible that the reported improvement over an equivalent conventional Si MOSFET may be largely attributable to the use of undoped silicon in the cap.

Clearly, based on the foregoing results, the cap layer should be made as thin as possible. However, a minimum value may be determined by two primary limitations; avoidance of high interface state densities (a minimum thickness of Ge-free silicon of order 6nm may be required [11]) and the avoidance of remote carrier scattering (by the insulator-semiconductor interface). Some experimental evidence suggests the latter may require a cap layer thickness of the order of 10nm [12] [13]. To enable significant benefit to be gained from the use of buried strained layer channels in sub-micron MOSFETs, two options exist - increase the offset potential between the cap and channel layers or reduce the peak field in the semiconductor. Growth of the HMOSFETs on silicon-on-insulator (SIMOX) substrates is one approach to field reduction [14], but, because of the heightened technological demands, does not appear to be a near term solution. Modulation doping provides one alternative.

Pulsed Modulation Doping.

It has been shown experimentally that a 'pulse' or 'delta' doped acceptor layer in the spacer below (but in close proximity to) the SiGe channel allows the inversion layer carrier concentration in the SiGe to be increased [11] [15]. In addition, the pulse doping layer reduces
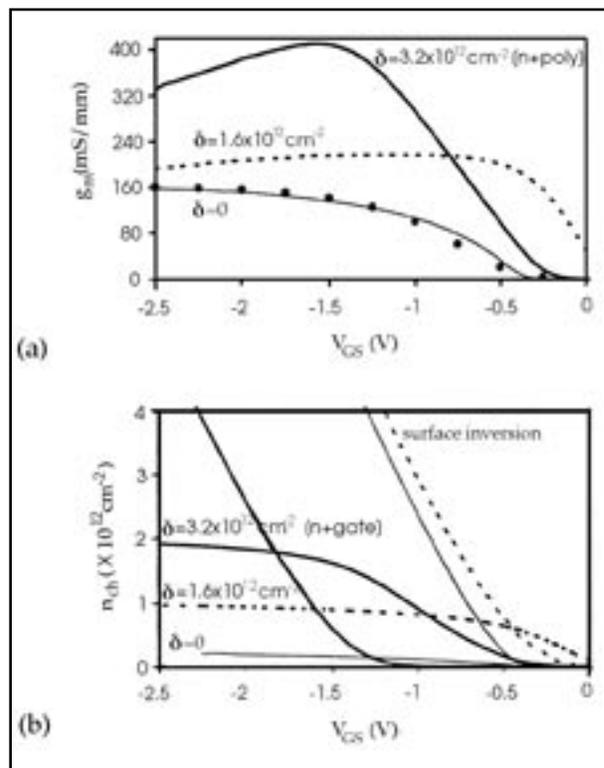

Figure 6.

(a) Transconductance curves obtained by simulation for an experimental 0.25µm gate length p-HMOSFET [9] with and without delta doping (V_{DS}=-2.5V). Dots represent experimental results.

(b) The inversion layer hole concentrations without delta ($\square$) doping layer (full line) and with a $\square$-dose of 0.8×10^{12} cm^{-2} (dotted).

the threshold voltage for inversion of the channel and increases ΔV_{GS}. Figure 6(a), shows that the inefficient device with a 7nm thick cap and effective gate length of 0.25µm (N_{sub} of 5 X 10^{17} cm^{-3}) is enhanced by the addition of 4nm thick pulse doping layers (of varying dose) set back 4nm below the channel. Peak transconductance improves from 144 mS/mm to 268 mS/mm and ΔV_{GS} from 0V to 0.4V as the sheet dose is raised from 0 to 2.0 X 10^{12} cm^{-2}. This very significant increase in gm(max) demonstrates the improvement in performance possible through epitaxial growth capabilities, such as in-situ modulation doping, quite apart from gains achieved by further increasing mobility. A δ-dose of 3.2×10^{12}cm^{-2} increases g_m to a value in excess of 400 mS/mm, remarkably high for any type of p-channel FET. Note that in this case, an n+ polysilicon gate is required to ensure enhancement mode operation (negative V_T), in the same manner as for a conventional buried channel p-MOSFET.

The increase in ΔV_{GS} is largely due to the reduction in transverse field achieved by the presence of the fully depleted pulse doped layer. This effect is the same as that proposed in the use of a 'back junction' [16] to modify the transverse field but in this case, excessive source-drain leakage in the off state (not shown) is avoided as long as the pulse doped layer is fully depleted.

Summary

As MOSFET gate lengths are shrunk to deep sub-micron dimensions, dopant concentrations in the channel region are forced higher to suppress short channel effects (~6×10^{17} cm^{-3} and 1×10^{18} cm^{-3} for 0.25µm and 0.12µm channel lengths respectively). 2d device simulation shows that it becomes ever more difficult to ensure inversion of a buried channel layer in HMOSFET devices with these levels of (sub channel) doping. This trend must be offset by employing maximum offset potentials at the cap-channel interface and minimum cap layer thicknesses. The same argument applies to n-channel HMOSFETs based on strained Si layers on SiGe. In the limit, this would suggest the use of Si (n-) and Ge (p-) channels for CMOS based on a relaxed Si$_{1-x}$Ge$_x$ (x≈0.5) virtual substrate. Modulation doping using pulse doping layers below the strained channel is a useful approach to extending the range of gate voltage over which conduction along the strained channel dominates. Indeed, this may prove essential if improved current drive and transconductance are to be realized in ultra-small geometry devices.

This article is based on material to be published in Microelectronics Journal.

References.

[1] K. Ismail, J.O. Chu and B.S. Meyerson, Appl. Phys. Lett., 64 (1994) 3124.

[2] Silvaco International, User Manual Edition 2, (1994).

[3] R. People, Physics and applications of GeSi/Si strained-layer heterostructures, IEEE J. Quantum Electron., QE-22 (1986) 1696.

[4] J. M. Hinckley and J Singh, Hole transport theory in pseudomorphic SiGe alloys grown on Si(001) substrates, Phys. Rev. B, 41(5) (1990) 2912.

[5] T. Manku, J. M. McGregor, A. Nathan, D.J. Roulston, J-P. Noel and D.C. Houghton, Drift hole mobility in strained and unstrained doped SiGe alloys, IEEE Trans. Electron Devices, ED-40 (1993) 1990.

[6] D.K. Nayak, J.C.S. Woo, J.S. Park, K-L. Wang and K.P. MacWilliams, Enhancement-mode quantum-well GeSi PMOS, Electron Device Lett., 12 (1991) 154.

[7] C. H. Gan, J. A. DelAlamo, B. R. Bennett, B. S. Meyerson, E. F. Crabbe, C. G. Sodini and L. R. Reif, Si/SiGe valence band discontinuity measurements using a semiconductor-insulator-semiconductor (SIS) heterostructure, IEEE Trans. Electron Devices, ED-41 (12) (1994) 2430.

[8] C. Lombardi, S. Manzini, A. Saporito and M. Vanzi, A physically based mobility model for numerical simulation of non-planar devices, IEEE Trans. Computer-Aided Design, CAD-7 (11) (1988) 1164.

[9] V.P. Kesan, S. Subbanna, P.J. Restle, M.J Tejwani, J.M. Aitken, S.S. Iyer and J.A. Ott, High performance 0.25?m p-MOSFETs with silicon-germanium channels for 300K and 77K operation, IEDM Tech. Dig., 91 (1991) 25.

[10] S. Verdonckt-Vandebroek, E.F. Crabbe, B.S. Meyerson, D.L. Harame, P.J. Restle, J.M.C. Stork, A.C. Megdanis, C.L. Stanis, A.A. Bright, G.M.W. Kroesen and A.C. Warren, SiGe-channel heterojunction p-MOSFETs, IEEE Trans. Electron Devices, ED-41(1) (1994) 90.

[11] S.S. Iyer, P.M. Solomon, V.P. Kesan, A.A. Bright, J.L. Freeouf, T.N. Nguyen and A.C. Warren, A gate-quality dielectric system for SiGe metal-oxide-semiconductor devices, IEEE Electron Device Lett., 12 (1991) 246.

[12] J. Ruolian, L. Jianlin, Z. Youdou, L. Haifeng and Z. Houzh, Hole transport properties of Si/SiGe modulation doped heterostructures, Superlattices and Microstructures, 16(4) (1994) 375.

[13] P.M. Garone, V. Venkataraman and J.C. Sturm, Mobility enhancement and quantum mechanical modeling in GeSi channel MOSFETs from 90 to 300 K, IEDM Tech. Dig. 91 (1991) 29.

[14] D.K. Nayak, J.C.S. Woo, G.K. Yabiku, K.P. MacWilliams, J.S. Park and K.L. Wang, High mobility GeSi PMOS on SIMOX, IEEE Electron Device Lett., EDL-14 (1993) 520.

[15] S.P. Voinigescu, P.B. Rabkin, C.A.T. Salama and P.A. Blakey, 2D numerical investigation of the impact of compositional grading on the performance of submicrometer Si-SiGe MOSFETs, IEEE Trans. Electron Devices, ED-42(6) (1995) 1039.

16] G.F. Niu, G. Ruan and T.A. Tang, Solid-State Electron., 38 (1995) 323.

Farewell to the 'Simulation Standard' ......
and Welcome to the "TCAD Driven CAD"
Family of Technical Journals

Silvaco is bidding farewell to the publication of our 'Simulation Standard' monthly technical journal. In five years of publication from June 1992 through June 1997, interest in this publication has been outstanding. Subscription in this period has grown significantly from 6000 to over 15,000 .

The 'Simulation Standard' has come to be recognized worldwide as a premier source of the latest information on advances in semiconductor technology modeling and simulation. With this publication, Silvaco has succeeded in its mission of providing continued updates on the latest technology advances to the semiconductor community worldwide. With the vast majority of all subscriptions now being delivered through direct mail, readers in all corners of the world now concurrently receive the latest technical information available. Silvaco would like to again express our appreciation to the many guest authors from industry and academia whose outstanding contributions have helped build this publication to the industry leading stature that it now enjoys.

As Silvaco continues to evolve as a company, the time has now come to expand the focus of our monthly technical publication. A new family of journals will be launched in July 1997 under the banner of 'TCAD Driven CAD'. The new publication will consist of three distinct issues, each published once quarterly. The new publication schedule is as follows:

"Journal for Process and Device Engineers"
February, May, August & November

"Journal for Circuit Simulation and
Spice Modeling Engineers""
January, April, July, October

"Journal For IC CAD/CAE Engineers""
March, June, September & December

This series of journals will provide both the leading edge technology coverage our readers have come to expect, and expanded coverage on the rapidly emerging integration of TCAD and traditional CAD in all phases of IC design. Readers can continue to look to Silvaco for unique insight into the technology issues that drive the development and manufacturing of next generation IC designs.

Design Automation Conference (DAC) Review

At DAC '97 Silvaco introduced the new pioneering TCAD Driven CAD product philosophy. A clear roadmap was presented for the continued development of Silvaco's software products which will deliver the power of the physical models from TCAD to the entire IC design process. Over the three days of exhibits there was tremendous interest in both the expanded product framework and the new tools that were introduced at the show. Over 500 demos were given on the interconnect parasitic extraction, IC design and verification, and analog circuit simulation products.

Among the new products introduced at the show were EXACT™ (interconnect parasitic extraction for process dependent test structures) and CLEVER™ (interconnect parasitic optimization for cells). These two products, which are both based on Silvaco's advanced 3D process simulation and 3D electrical field solver, allow users to accurately model the impact of process variations on the parasitics of a wide variety of interconnect

structures. Visitors at DAC were quick to agree that this unique process based approach to parasitic extraction is the only solution available that meets the rigorous accuracy demands of sub-quarter micron IC design. These products are now available from Silvaco.

Also introduced at DAC were the first in a series of Windows NT-based IC CAD tools. Expert(tm) (high performance ULSI layout editor) and Savage(tm) (fully integrated hierarchical design rule checker) were demonstrated for visitors at DAC. The level of performance of these products was seen to meet or exceed that of industry leading UNIX based products. With data structures common to the entire TCAD Driven CAD framework, these products uniquely offer a linkage with the TCAD physical models that allow designers to quickly and easily evaluate the impact of design changes on the performance, reliability and manufacturability of the complete design.

Calendar of Events

June

1
2
3
4   Blaze Workshop - Italy
5
6
7
8
9   DAC 97 - Anaheim, CA
10 DAC 97 - Anaheim, CA
11 DAC 97 - Anaheim, CA
    Workshop - Scotland
12 Workshop - Munich
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27 Workshop - Japan
28
28
30

July

1
2
3   Workshop - Guildford
4
5
6
7
8   Workshop - Munich
9   Workshop - Japan
    Workshop - Grenoble
10 Workshop - Japan
11 Workshop - Japan
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
28
30
31

Bulletin Board

Silvaco International Taiwan Opens for Business!

To support the rapidly growing South East Asian market Silvaco International has opened our own dedicated support and training center. The office is conveniently located right next to the main entrance gate of the Science Based Industrial Park in Hsinchu.

The address is:

Silvaco International
472 Kuang-Fu Road, Section 1
8th Floor, Unit 3
Hsinchu, Taiwan

Summer '97 Release of ATHENA and ATLAS!

A major release of ATHENA and ATLAS is now available on CD ROM. All currently maintained customers have been updated. If you wish to receive or evaluate the latest development in process and device simulation, contact your local Silvaco representative.

Silvaco Furthers Collaboration with University of Surrey!

Silvaco International, University of Surrey (represented by Dr. Rodger Webb) and Applied Material UK have agreed to collaborate on the development and characterization of next generation 2D and 3D ion implantation modeling. University of Surrey is recognized as the center of excellence for Ion Beam Technologies. Models derived from this work will be SIMs verified over wide range of energies, angles and dozes. The measured profiles will be available to customize through SPDB product.

Silvaco Development Staff Grows!

Contrary to recent press reports, that inaccurately portrayed Silvaco's development staff as "minuscule", we have done an in-depth R&D study which has conclusively shown that at a mean height of 5'10" Silvaco's development staff comfortably ranks in the top 5% of all EDA companies.

For more information on any of our workshops, please check our web site at **http://www.silvaco.com**

Hints, Tips and Solutions

Andy Strachan, Applications and Support Manager

Q: How can I determine implant range for non-standard materials such as silicides or photoresist?

A: The analytical implant tables in ATHENA/SSuprem4 cover implantation of the common silicon dopants (B, P, As, Sb, In) into the commonly used set of materials in semiconductor processing (Silicon, SiO_2, Si_3N_4, polysilicon, aluminum). For other materials or implant species the lack of complete data means full analytic tables are not available. The only alternative approach was to use Monte Carlo (MC) Implant simulation.

Implantation using MC with the crystalline model is usually required for silicon implantation. For realistic 2D cases these implants may take up to 30 minutes to run on a Sparc Ultra. In order to overcome this problem an alternative approach is now available in ATHENA version 4.3. This approach uses MC implant in 1D mode to run implantation simulations into the material of interest. Then the analytical implant moments are extracted from the implanted doping profile. These analytical moments can be used in a MOMENTS statement to set the correct doping profiles for an analytical implant. The syntax for this is shown in Figure 1 with a comparison of the two different implants in Figure 2.

Photoresist is a special case in ATHENA. Although analytical implant tables exist for photoresist, they are specific only to one type of photoresist (AZ-111). Photoresist materials
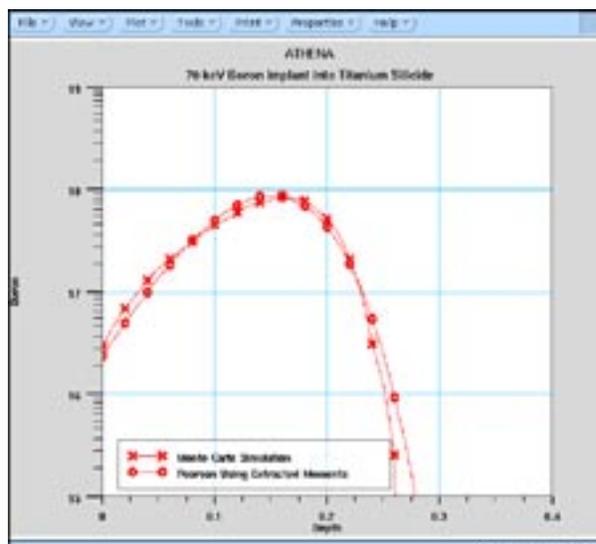

Figure 2. Comparison of doping profiles analytical extraction versus Monte Carlo. Analytical implants are run instantaneously whereas Monte Carlo takes up to 30 minutes on Ultrasparc.

do vary considerably in density and material abundances. Syntax exists in ATHENA to set the required parameters for MC implantation modeling.

```
MATERIAL   MATERIAL=my_resist DENSITY=3 \
          ABUND.1=0.6 AT.NUM.1=8 AT.MASS.1=16 \
ABUND.2=0.4 AT.NUM.2=6 AT.MASS.2=12
```

ABUND sets the relative abundance of elements in the photoresist. AT.NUM and AT.MASS set the atomic number and weight of the elements respectively. DENSITY sets the overall material density. From these parameters, MC implant can calculate the implanted profile. The syntax from Figure 1 allows the user to fit, extract and re-use the analytical moments calculated from the MC implant profile.

A similar technique can be used for implants of non-standard species too. It is possible for users to build up their own user-defined implant moment tables. An example of the use of this technique is included on the Summer 97 release CDROM with ATHENA version 4.3.

Figure 1. Syntax for extracting analytical implant parameters from a Monte Carlo implant simulation.