Simulation Standard

SILVACO International

A Journal for Process and Device Engineer

Performing Optical Proximity Correction (OPC) in ATHENA

Introduction

One of the main goals in lithography processes is to transfer the pattern on the photomask onto the wafer surface as accurately as possible. However, due to the diffraction from the edges and the interference between neighboring mask features, the mask pattern and its printed image are bound to be different. As shown in Figure 1, corner rounding, line shortening and non-uniform linewidth are few of the proximity effects that have been observed. For a binary mask, making small modifications on the mask pattern by adding serifs to the corners and by moving the pattern boundaries are the basic vehicles in counteracting these proximity effects. In conjunction with *MaskViews* and *TonyPlot*, *Optolith* has been extended to perform optical proximity correction (OPC). This new OPC capability will enable the process engineer to examine various aspects of the proximity effect on the lithography process window. Details of these enhanced tools are discussed in the following sections.

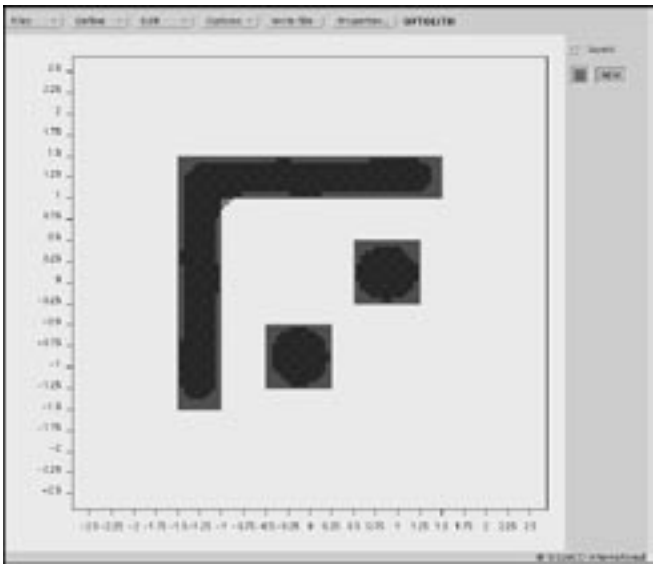

Figure 1. The image from a mask does not match the intended layout. Importing the aerial image into MaskViews acts as a guide for OPC.

The OPC Tools

The procedure to performing OPC is similar to simulating the aerial image of a given mask pattern. Use *MaskViews* to draw or to import the layout file, and then use *Optolith* to calculate the aerial image. Visualization of the image profile is done in *TonyPlot*. If the deviation between the image and the pattern is not acceptable, the layout pattern can be modified and these steps repeated. To achieve the final corrections on the mask pattern, several iterations may be required. In order to expedite the process, special features have been incorporated into the above mentioned interactive tools.

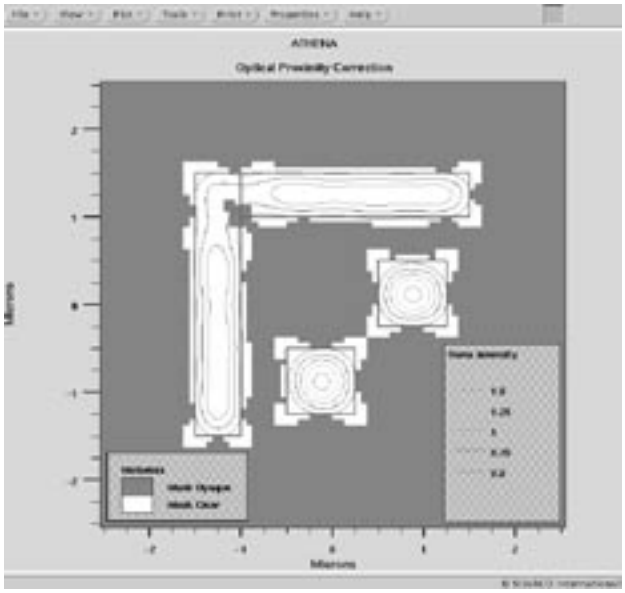

Figure 2. Outline of the unbiased mask pattern overlayed with the layout and image of the biased mask.

MaskViews Enhancements

As a visual guide for the user in making correction to the mask layout, *MaskViews* can now import the aerial image output file from *Optolith* and then overlay it onto the mask pattern [Files-Import-Optolith format], see

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INSIDE

Figure 1. Furthermore, a new serif object has been created [Define-Objects-Object] to let users to adjust the size of the serif. Adding user-defined serifs to the corners of a mask feature is done just at the push of a button [Edit-Add serifs].

***Optolith* Enhancements**

In designing this OPC generator, we have assumed a threshold model in the response of the photoresist to the energy dosage, which means the chemical characteristics of the positive photoresist will change above a user-defined threshold level. The normalized intensity threshold level is specified by the opc-option as in the following statement,

```
structure outfile=anopex252.str /
infile=anopex25.sec opc=0.5
```

This syntax also signifies *ATHENA* to search for an layout section file anopex25.sec, generated by *MaskViews* for the unbiased original mask layout, and to include the information of the unbiased mask into the output structure file for later use in *TonyPlot*. This unbiased mask pattern is required for calculating the percentage of the area of the mask pattern that is below the threshold level (AB), and the percentage of the image area that is lying outside of the mask pattern (AO). These are defined as,

$$AB = \frac{\text{area of the mask pattern that is below the threshold level}}{\text{total area of the mask pattern}} \times 100\%, \quad (1)$$

and

$$AO = \frac{\text{area of the image lying outside of the mask pattern}}{\text{total area of the image}} \times 100\%, \quad (2)$$

It is our belief that these two figures of merit are much easier to calibrate than the distribution of distance deviation. For the unbiased mask shown in Figure 1, AB and AO are equal to 32.4% and 0.7%, respectively. For the corrected mask displayed in Figure 2, AB and AO become 12.0% and 3.7%, respectively. There is approximately 20% improvement in filling up the mask pattern. A cross-section of the intensity profile, Figure 3, reveals that the image of the corrected mask not only conforms better to the ideal case, but also has a better contrast and steeper slope. These are very good indications that OPC will be able to enlarge the existing process window without using the phase-shifting mask technology or demanding for more exotic optical system and light source. The potential advantages for the semiconductor industry are tremendous extending the lifetime of the existing process equipment and knowledge base, and reducing the pressure on new process technology development, to name a few.

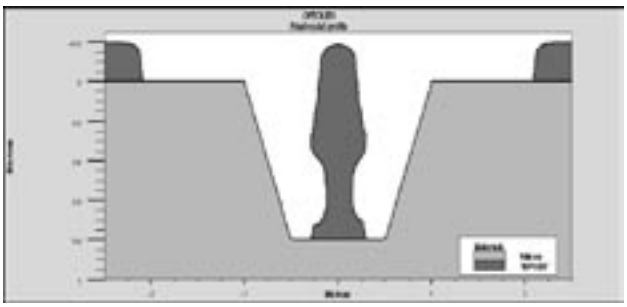

Figure 4. Note the reflective notching effect at the lower half of the photoresist profile inside the trench.

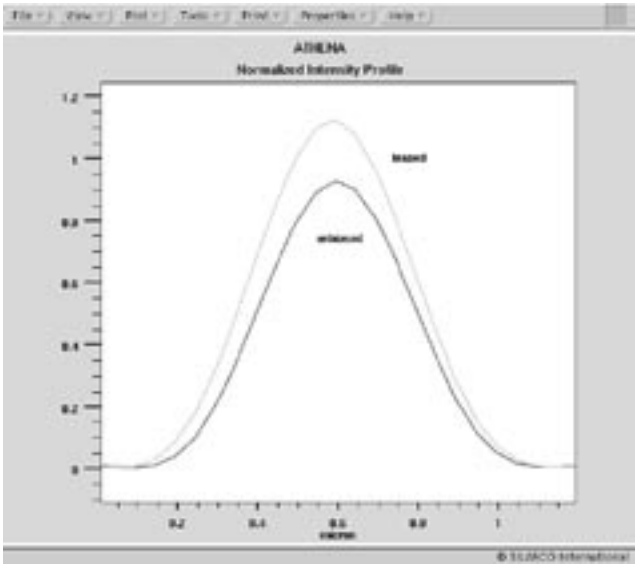

Figure 3. Image intensity profiles for the biased and unbiased mask.

Besides calculating the two figures-of-merit, an image output file is automatically generated for *MaskViews* to overlay with the mask layout as mentioned above. The filename of the image file has the following syntax: x_img.sec, where x is the filename specified in the outfile-option, for example, anopex25_2_img.sec.

***TonyPlot* Enhancements**

To give a visual inspection on the integrity of the image of the biased mask pattern, the outline of the unbiased mask layout can be drawn on top of the usual contour plot of the aerial image intensity profile.

Additional Optolith Improvements

In addition to the OPC capability, *Optolith* has been upgraded in two other aspects. Firstly, the speed in calculating the aerial image has been greatly increased without sacrificing the accuracy. This improved algorithm is slightly better than the n-log-n type technique. Secondly, the accuracy of the ray tracing technique employed in the photoresist exposure modeling has been enhanced. This technique is especially applicable to evaluate the latent image formation in the photoresist over a realistic nonplanar device geometry without rendering into other time consuming algorithms, for example, the time domain finite difference method [1]. The reflective notching effect from the sidewalls of the trench is clearly shown in the developed resist profile depicted in Figure 4.

Reference

[1] R. Guerrieri, K. H. Tadros, J. Gamelin, and A. R. Neureuther, IEEE Trans. Computer-Aided Design, 10, 1091-1100 (1991).

Simulation of Ion Irradiated Power Devices in ATLAS

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Introduction

About ten years of evolution was sufficient for ion irradiation technology to become a widely used tool for local carrier lifetime control in power devices. In 1994, the simulation of devices taking into account both the real defect profile resulting from ion irradiation and multi-level Shockley-Read-Hall model was published for the first time [1]. *ATLAS* has allowed simulation of transient traps since 1995 [2]. The last version of *ATLAS* (4.0) brought the possibility to account for arbitrary defect spatial distribution. So the development of ion irradiated devices using device simulation is now possible [3]. At present, any application of the simulator requires just a knowledge of the spatial distribution of the defects resulting from irradiation and electrical parameters of the related deep levels [4]. The practical application of this will be presented below for the case of power diode.

Background

Deep levels generated by ion irradiation affect the free-carrier thermal generation-recombination and hence the excess carrier lifetime. The thermal capture and emission of carriers through deep levels located within the bandgap is described in *ATLAS* by analytical model based on SRH statistics. In case of k independent single-charged acceptor- or donor-like levels the thermal components of the recombination rates R_n and R_p for electrons and holes, are respectively [1-3]:

$$R_n = \sum_{i=1}^{k} \left[K_{ni} \cdot N_{ti} \cdot (1-f_i) - G_{ni} \cdot N_{ti} \cdot f_i \right]$$

$$R_p = \sum_{i=1}^{k} \left[K_{pi} \cdot N_{ti} \cdot f_i - G_{pi} \cdot N_{ti} \cdot (1-f_i) \right]$$

where N_{ti} is the concentration of the i-th deep level and $G_{n(p)}$ and $K_{n(p)}$ are the i-th level emission and capture rates for electrons (holes). The electron occupancy f_i of the i-th deep level is calculated from the following balance equation

$$\frac{df_i}{dt} = K_{ni} \cdot (1-f_i) - G_{ni} \cdot f_i + G_{pi} \cdot (1-f_i) - K_{pi} \cdot f_i$$

The charge of traps $D_t=(p_t-n_t)$ influences the right-hand side of the Poisson equation

$$\varepsilon \nabla^2 \Psi = -q \, (p - n + N_D^+ - N_A^- + p_t - n_t)$$

Application of this model requires a detail knowledge of deep level parameters. The *ATLAS* command is

```
doping trap ascii inf=… acceptor/donor  \
e.level=... sign=… sigp=… degen=…
```

ATLAS also incorporates a model for transient trapping and de-trapping of carriers. For dynamic equilibrium $df_i/dt=0$ (DC analysis) CPU time is saved because the recombination rate R is unique and may be expressed explicitly by one equation in the following way

$$R_n = R_p = \sum_{i=1}^{k} N_{ti} \cdot \frac{n \cdot p \cdot K_{ni} \cdot K_{pi} - G_{ni} \cdot G_{pi}}{K_{ni} \cdot n + K_{pi} \cdot p + G_{ni} + G_{pi}}$$

Transition between the two states is automatic in *ATLAS*. There is available a second SRH model (`models srh`) which uses the static approximation even for transient analysis. In this case only a single G-R centre is considered and the equation above leads to the fairly well known formula

$$R_t = \frac{n \cdot p - n_i^2}{\tau_{p0} \cdot \left[n + n_i \cdot exp\left(\frac{E_t - E_i}{kT}\right) \right] + \tau_{n0} \cdot \left[p + n_i \cdot exp\left(\frac{E_i - E_t}{kT}\right) \right]}$$

where k is Boltzmann constant, T is the temperature, n_i is intrinsic concentration, E_i intrinsic Fermi-level, E_t trap level, $\tau_{n(p)0}=1/(\sigma_{n(p)}.v_{n(p)}.N_t)$ are electron and hole lifetimes, resp. It is worth reminding that this equation is true only for a single ideal G-R center ($R_n=R_p$) or dynamic equilibrium, (e.g. ON- or OFF-state).

Defining Trap Parameters

The device under consideration is a p^+pnn^+ power diode (2.5kV/100A) with length of 370μm between anode and cathode. The detailed device data may be found in [5]. In order to present the simulation capabilities of *ATLAS* the device under test was virtually irradiated by 10 and 18 MeV $^4He^{2+}$ ions with the dose of $5x10^9$ cm^{-2} using the calibrated system for determination of defect distribution [1]. The parameters of deep levels created by penetrating ions were determined by means of the deep level transient spectroscopy (DLTS) and are summarized in Table 1 using the notation of *ATLAS*. Helium irradiation produces pure damage defects comprising five deep levels within the bandgap which are connected with different charge states of divacancy (E2, E3, H1), acceptor level of vacancy-oxygen VO pair (E1), and donor level of the carbon-vacancy-oxygen CVO complex (H2). The data received from measurements for level positions E_t

Acceptor-like traps					Donor-like traps				
Trap	E.LEVEL (eV)	sign (cm^2)	sigp (cm^2)	Identity	Trap	E.LEVEL (eV)	sign (cm^2)	sigp (cm^2)	Identity
E1	0.165	6×10^{-15}	3.4×10^{-13}	VO (0/-)	H1	0.195	5.5×10^{-15}	5.1×10^{-16}	V_2(0/+)
E2	0.23	1.5×10^{-15}	5.5×10^{-14}	V_2 (-/=)	H2	0.356	2.3×10^{-15}	3×10^{-16}	COV(0/+)
E3	0.42	4.7×10^{-15}	2.8×10^{-14}	V_2 (0/-)					

Table 1. Deep levels in FZ n-type silicon irradiated by $^4He^{2+}$ ions.

(E.LEVEL) and electron capture cross-sections *sign* were completed by capture cross-sections for holes *sigp* presented in reference [4] for the same type of defects.

The influence of individual deep levels on electron lifetime is shown in Figure 1 for both the defect peak (x~180μm) and defect tail (50μm<x<150μm) regions of the 18 MeV irradiation (see Figure 2) using the general lifetime dependence on excess carrier concentration that reads

$$\tau_n = \frac{\Delta n}{R_n}$$

The thermal component of R_n was calculated from the first equation above for deep level parameters given in Table 1. Figure 1 enables one to compare the lifetime reduction in the defect peak with both the unirradiated region and tail part. Furthermore, $\tau(\Delta n)$ as a result of individual and all deep levels implies that only two levels are dominant.

The level E1 has the biggest impact on the lifetime decrease with increasing excess carrier concentration above 10^{14} cm^{-3} and determines the so-called high-level lifetime. The level E3 is counteracting, so it dominates in decreasing the lifetime below 10^{14} cm^{-3} . This is usually referred as a low-level lifetime. For the device under consideration, the E1 level is responsible not only for the magnitude of the DC forward voltage drop ($n > 10^{15}$ cm^{-3}), but also for the excess carrier recombination within the neutral n-base during the initial part of the turn-off. E3 brings mainly the desirable decrease of charge at the far end of reverse recovery ($n > 10^{15}$ cm^{-3}). Finally, the figure implies the fact that simulation with the two dominant levels (E1 and E3) gives the same results as with five ones (verified in simulations of reverse recovery). Since the influence of both the double-acceptor (E2) and single donor (H1) levels of divacancy is marginal, the defect can be approximated as a single acceptor E3. Therefore, a problem with inclusion of multiple-charged centers, which are not covered by the current *ATLAS* SRH model, is avoided.

Device Simulation

Figure 2 shows the excess carrier distribution $n + p$ of both the unirradiated and helium irradiated devices during the ON-state (100A@300K). Figure 3 shows the reverse recovery current and voltage waveforms to be simulated for dc reverse voltage -1000V and dI/dt=-1000A/μs starting from the conditions of Figure 2. The overall behavior of irradiated devices is influenced by position of the defect peak (ion energies) that was intentionally located in two places with different impact on

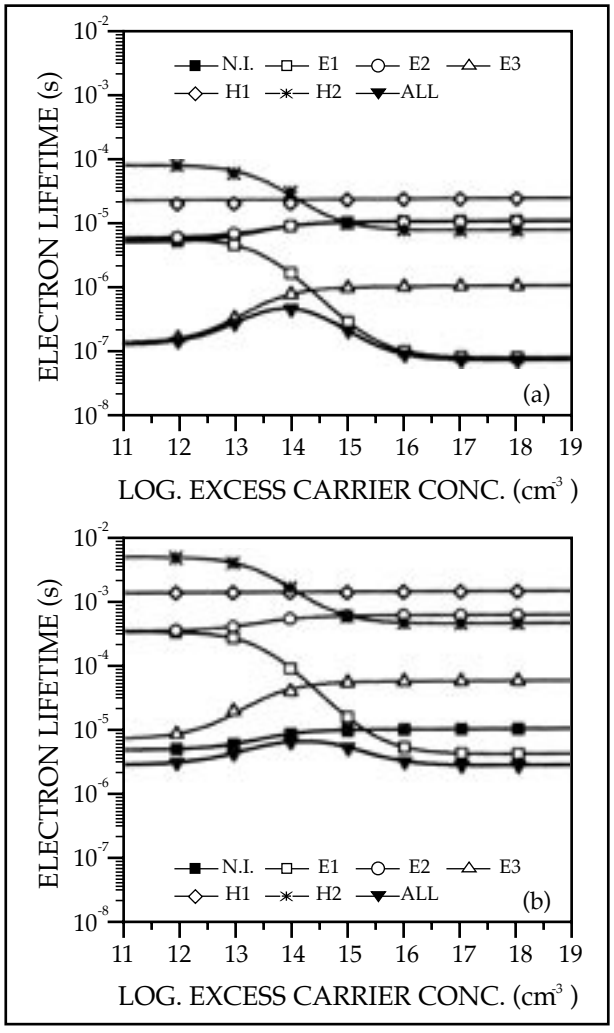

Figure 1. Electron lifetime at defect peak (top) and tail (bottom) vs. injection level ($\Delta n = \Delta p$, static approx., T = 300 K, N.I. = no irradiation, ALL=all levels accounted for)

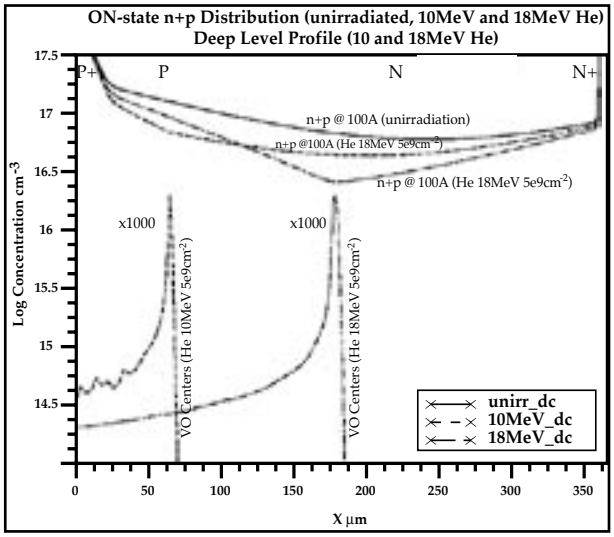

Figure 2. The profile of VO centers generated by 10 and 18 MeV He^{2+} $5x10^9$ cm^{-2} irradiation and ON-state sums of carrier distributions n+p for unirradiated and irradiated diode (I_f = 100A).

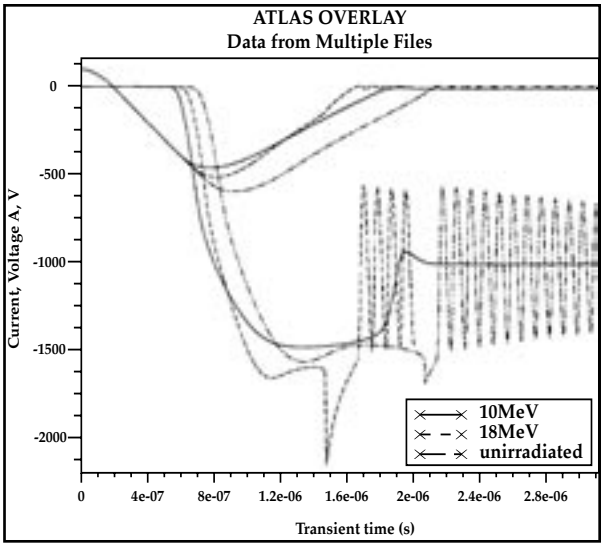

Figure 3. Current and voltage waveforms of the reverse recovery process (VRM= -1000V, dI/dt= -1000A/ms) for unirradiated and He irradiated diodes (10 and 18MeV@$5x10^9cm^{-2}$)

device parameters. The forward voltage drop V_F is 0.94, 0.98, and 1.032V @100A for unirradiated devices, 10MeV and 18MeV (dose: $5x10^9cm^{-2}$) irradiations, respectively. The gradual increase of V_F with defect peak distance from the anode is in agreement with experiment [5]. The influence of ion irradiation on dynamic behavior is more pronounced. While the unirradiated device shows oscillators, the 18MeV one is even worse. On the other hand, using 10MeV the defect peak placed within the n-base close to the anode softens the diode recovery in agreement with experiment [5]. As a result the removal of the oscillatory behavior takes place.

Conclusions

It was shown that *ATLAS* is capable of accurate simulation of ion irradiated power devices. The user should provide the electrical parameters of relevant deep levels and define trap models accordingly in the *ATLAS* syntax.

References

[1] Hazdra P., Vobecky J., "Accurate Simulation of Fast Ion Irradiated Power Devices", Solid-State Electronics, Vol. 37, No. 1, pp. 127-134, 1994.

[2] ATLAS User's Manual, SILVACO International, June 1995

[3] ATLAS User's Manual, SILVACO International, October 1996

[4] Hallén A., Keskitalo N., Masszi F., Nágl V., "Evaluation of Local Lifetime in Proton Irradiated Silicon", J. Appl. Phys., Vol.79, pp.3906 - 3914, 1996

[5] J. Vobecky, P. Hazdra, and J. Homola, "Optimization of Power Diode by Means of Ion Irradiation", IEEE Trans. on Electron Devices, Vol. 43, pp.2283 - 2289, 1996

Simulation of Silicon Germanium HBTs Using ATLAS/BLAZE

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The aim of this technical report is to study the suitability of *ATLAS/Blaze* for the simulation of state-of-the-art high-speed SiGe heterojunction bipolar transistors (HBTs) fabricated in close-to-conventional Si-technology. Simulation studies of advanced SiGe HBTs are presented and, where possible, verified with experimental results.

Material Parameters

The incorporation of germanium significantly changes the properties of the base region and the base-emitter and base-collector junctions in a $Si/Si_{1-x}Ge_x/Si$ HBT. Addition of Ge reduces the bandgap of Si, leading to the narrow bandgap SiGe base of the HBT. The lattice constant of $Si_{1-x}Ge_x$ alloy differs considerably from that of Si . Hence, the incorporation of Ge causes strain in the SiGe (compressive in-plane), modifying the energy band structure and density of states in the conduction and valence bands.

The quality of epitaxially grown SiGe/Si heterostructures has improved dramatically in recent years and reported results are very promising in terms of the possibilities offered by the SiGe technology. However, while silicon has been well-characterized over the past 40 years, not nearly as much is known about strained SiGe and many simplifying assumptions are made in the strained-SiGe/Si material parameters.

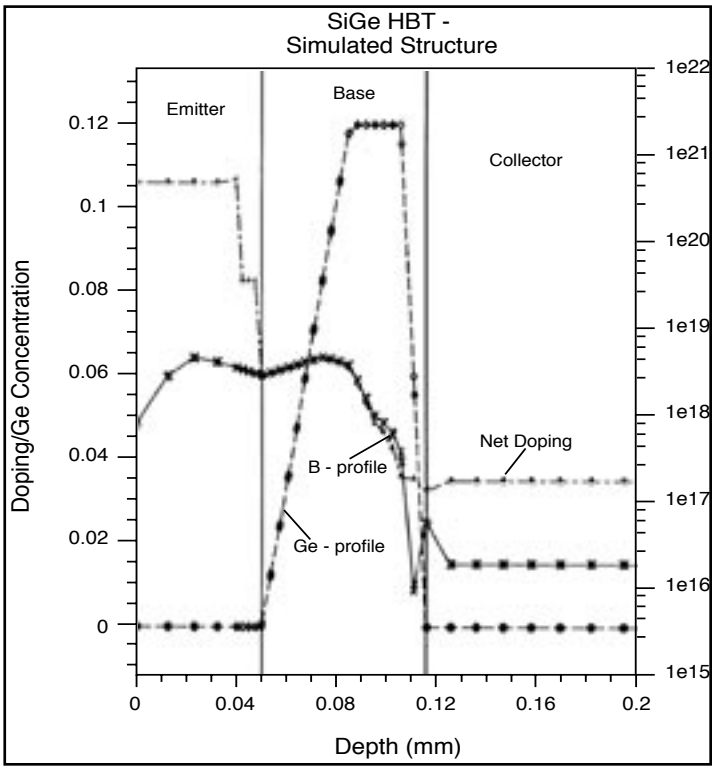

Figure 1. Doping profile and Ge profile (graded base) of a SiGe HBT. Based on Meister et. al. IEDM 95 p. 739.

Simulation of Advanced SiGe HBTs

Since the introduction of SiGe into conventional Si technology, various research groups have demonstrated high performance SiGe base HBTs with different approach to forming the Ge profile in the base. While the IBM group [1] uses graded Ge profiles, the Daimler Benz group [2] focuses on SiGe HBTs with a uniform Ge profile. Recently Harame et al. [1] have developed a high-performance SiGe-base BiCMOS process.

The highest speed (f_{max}) SiGe transistor reported so far appears to be by Schuppen et al. [2]. They used a relatively thick (60 nm) base and heavy doping to reduce the intrinsic base resistance. The base transit time was reduced by a strong electric field with 0 to 15% Ge grading. Meister et al. [3] have reported a SiGe HBT with a 74 GHz f_{max} , resulting in a record CML gate delay of 11 ps.

The key issue in this study was to investigate HBT structures which offered both high f_T and f_{max}. The simulation results have been compared with the latest reported experimental results [3] as summarized in Table 1. Figure 1 shows the simulated device structure where the Ge profile and doping profiles in various transistor regions

		Experimental	Simulation
Emitter Size	A_E	0.27 x 2.5 μm^2	0.27 x 2.5 μm^2
Current Gain	B	220	210
E-B Breakdown Voltage	B_{VEBO}	3.0	3.0
Early Voltage	V_A	130 V	110 V
Cutoff Frequency	f_T	61 GHz	63 GHz
Max. Osc. Freq.	f_{max}	74 GHz	110 GHz

Table 1. Comparison of simulated and measured data.

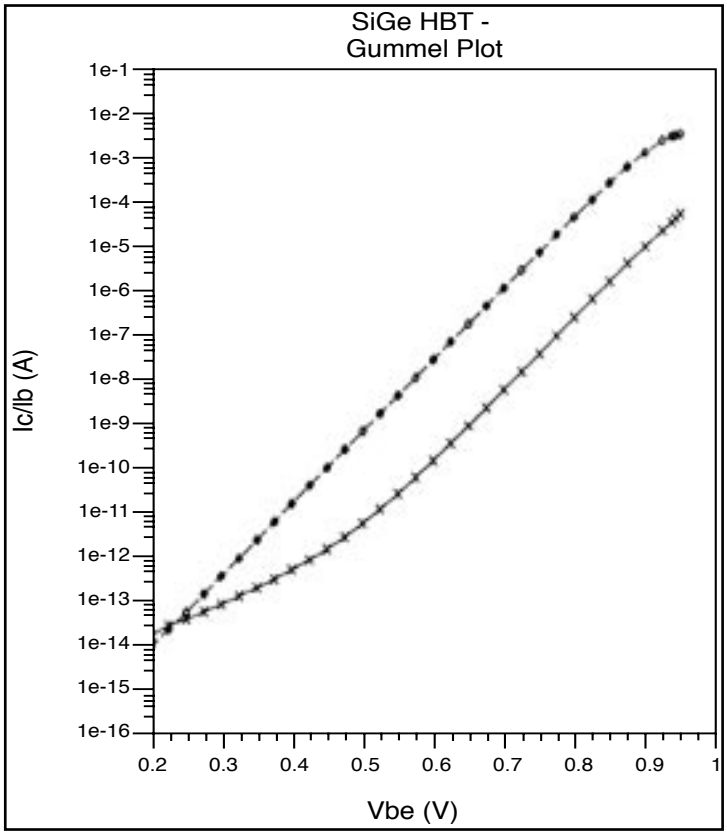

Figure 2. Gummel plot of a SiGe (graded based) HBT. Based on Meister et. al. IEDM 95 p. 739. [3].

are shown. The choice of this structure was made because of the availability of reliable experimental data for such a device.

The Ge concentration in the base has been graded from 0% at the emitter-base junction to 12% at the base-cellector junction. Figure 2 shows the Gummel plot and it is seen that almost ideal base current characteristics are observed. The transistor has a simulated peak dc current gain of about 210, as shown in Figure 3, which compares well with the experimental value of 220. The simulated cutoff frequency f_T is seen to be about 63 GHz while the calculated f_{max} has a value of more than 100 GHz, as shown in Figures 4 and 5 respectively.

In Figure 5 also shown are the small signal current gain β_{ac} extracted from h-parameters and the maximum available gain (MAG). From these curves a unilateral power gain of 22 dB at 10 GHz and an f_{max} of about 110 GHz (MAG) have been obtained at the reverse base-collector voltage of 2 V. In particular this high f_{max} value originates from the integration of the SiGe base, providing both high cutoff frequency and low intrinsic base resistance.

The effect of collector doping on the Early voltage V_A obtained from the simulated output characteristics (I_b = 15 nA) is shown in Figure 6. It is seen that as the doping concentration increases in the collector, the Early voltage decreases. For a collector doping of $5x10^{16}$ cm^{-3}, the predicted V_A is 110 V, giving a high $\beta.V_A$ product exceeding 22000. A Ge fraction of 12% at the base-collector junction has provided the high Early voltage.

Summary

Relatively simple material parameters for strained SiGe layers grown on Si(100) are incorporated in *ATLAS*/*Blaze*. The carrier mobility models in strained SiGe are very conservative and are similar to silicon. Mobility enhancements due to strain have not been modeled.

As more studies are performed on the electrical properties of SiGe strained layers, the program can easily be modified to include the latest findings. Simulation results for both silicon and SiGe bipolar transistors are in good agreement with reported experimental results available in the literature.

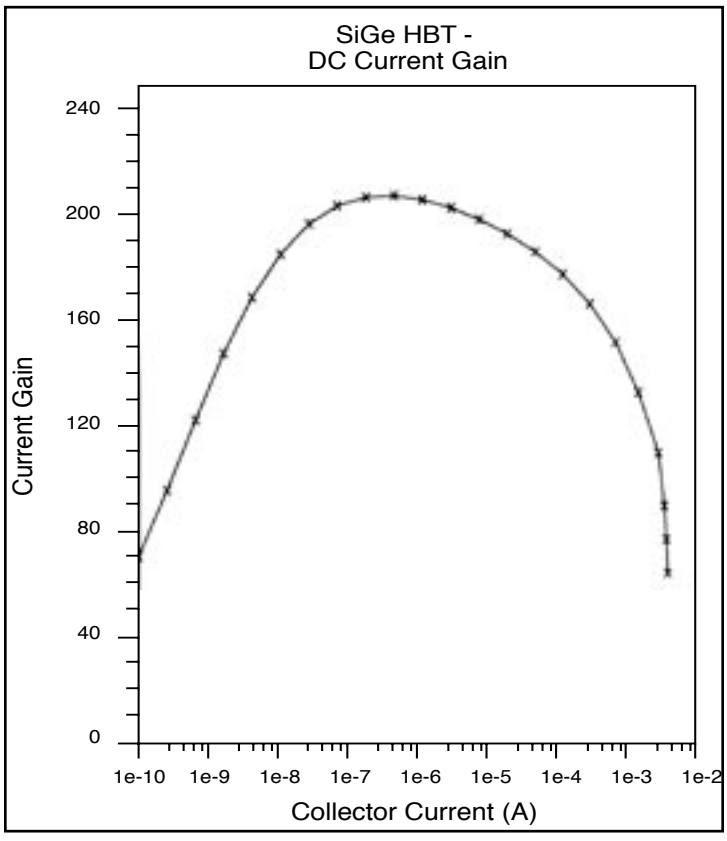

Figure 3. Simulated DC current gain of a graded base SIGe HBT. Based on Meister et. al. IEDM 95 p. 739.

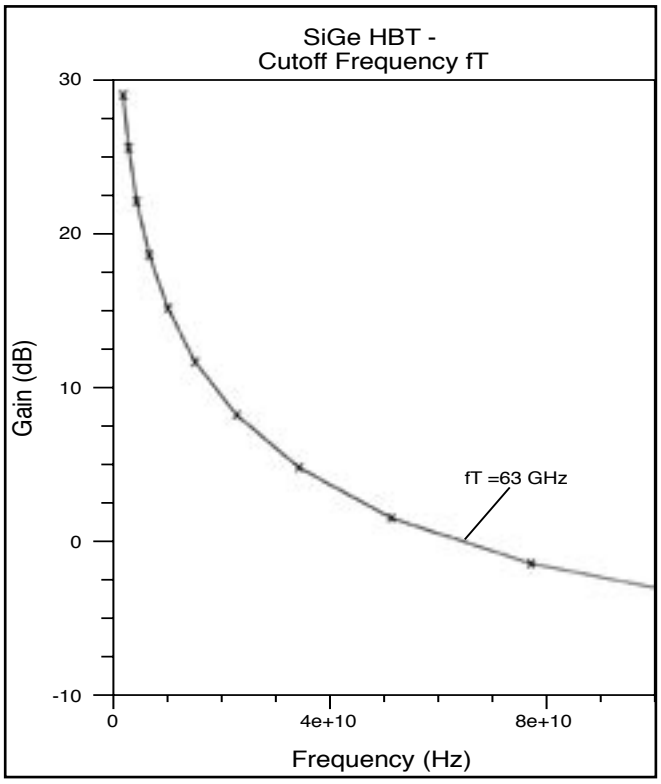

Figure 4. Simulated Frequency (f_T) of a graded base SiGe HBT. Based on Meister et. al. IEDM 95 p. 739.

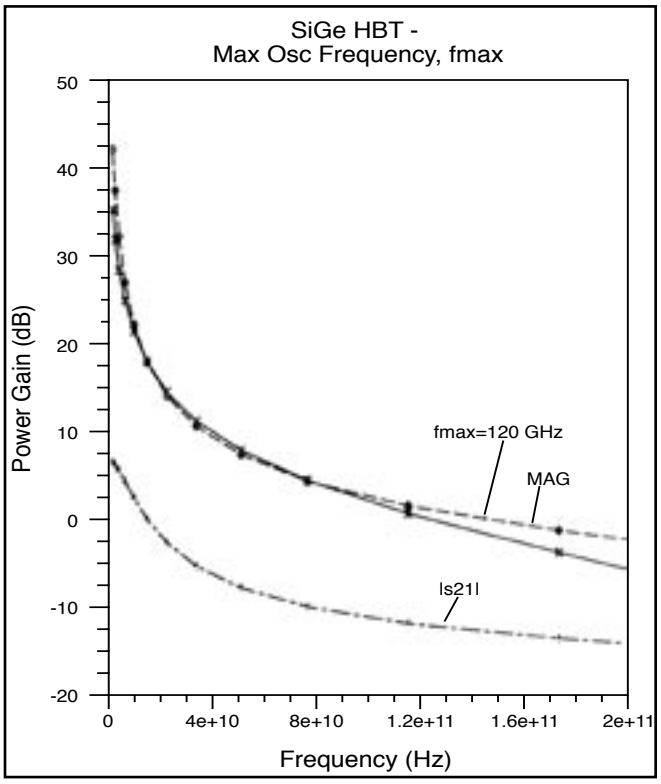

Figure 5. Simulated Frequency of Oscillation of a graded base SiGe HBT. Based on Meister et. al. IEDM 95 p. 739.

SiGe HBTs with a constant (flat) germanium concentration in the base have very large current gains but similar f_T to silicon devices. Unity gain cutoff frequency of over 63 GHz was simulated by *ATLAS* for a graded base SiGe HBT. This is consistent with experimental value of 61 GHz reported by Meister et al. [3]. The projected f_{max} was reported to be about 74 GHz and our simulation results give rather a more optimistic value of over 100 GHz.

References

[1] D. Harame et al., "SiGe HBT Technology: Device and Application Issues", IEEE IEDM Tech. Dig., pp. 731 - 734, 1995.

[2] A. Schuppen, U. Erben, A. Gruhle, H. Kibbel, H. Schumacher and U. Konig, "Enhanced SiGe Heterojunction Bipolar Transistors with 160 GHz f_{max}", IEEE IEDM Tech. Dig., pp. 743 - 746, 1995.

[3] T.F. Meister, H. Schafer, M. Franosch, W. Molzer, K. Aufinger, U. Scheler, C. Walz, M. Stolz, S. Boguth and J. Bock, "SiGe Base Bipolar Technology with with 74 GHz f_{max} and 11 pS Gate Delay, IEEE IEDM Tech. Dig., pp. 731 - 734, 1995.

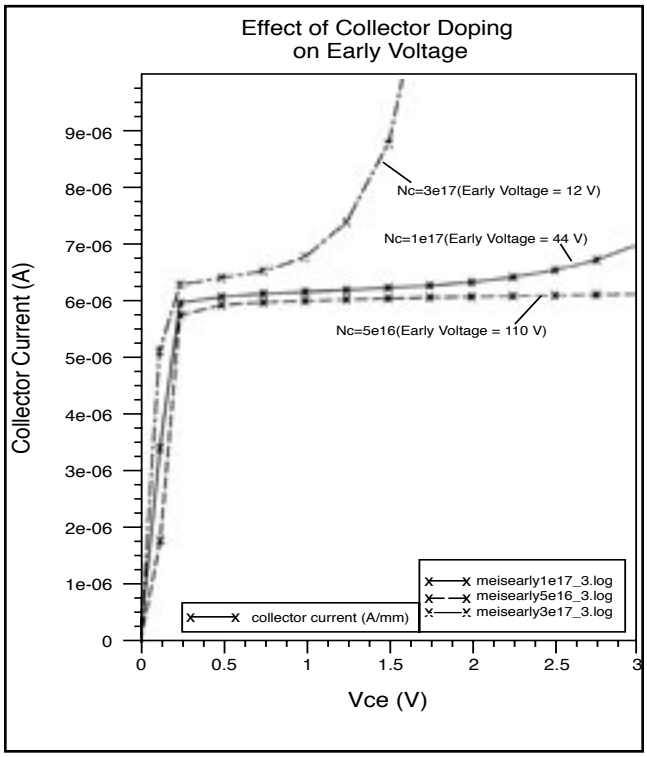

Figure 6. Typical simulated output characteristics of a graded base SiGe HBT as a function of collector doping. Based on Meister et. al. IEDM 95 p. 739.

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Bulletin Board

Visit Silvaco at SPIE 97!

Silvaco engineers will be presenting the latest advances in non-planar lithography simulation using ***Optolith*** at the "SPIE 1997 Symposium on Microlithography". This will be at the Santa Clara Convention Center from 10th to 14th of March. Lithography engineers will have the chance to view demonstrations of ***Optolith*** and the ***Virtual Wafer Fab***^{tm} including the OPC features described elsewhere in this issue.

See the latest in UTMOST, SPAYN and SmartSpice!

Demonstrations of the latest advances in SPICE modeling and simulation will be available at the IEEE Microelectronic Test Structures Conference. This will be held in the De Anza Ballroom lobby at the Doubletree Inn in Monterey, CA from the 18th to 20th of March. Characterization engineers will be able to view the latest in MOS, Bipolar and SOI SPICE model extraction and circuit simulation.

MixSim demonstration at IVC/VIUF!

Silvaco will be introducing ***MixSim,*** an innovative and powerful mixed-level / mixed-signal circuit simulator. ***MixSim*** provides the capability to simulate mixed signal circuits in the time domain using any combination of Verilog, Switch or Spice primitives. This conference will be held on April 1 & 2 at the Santa Clara Convention Center. Design and Verification engineers can meet with Silvaco's developers and application engineers and view hands on demonstrations of the product.

New Director of Sales for Central Europe!

We are pleased to welcome Andreas Schutte as our new sales director for central Europe based in the Munich office. He fills the post created by the recent move of Hans Sporrel to our European Headquarters in Guildford, UK. Andreas brings over 20 years experience in high tech international sales with companies such as HP and NCR. Returning to Germany after 12 years in the US, Andreas will play a key role in Silvaco's continued expansion in Europe. He can be reached by e-mail at andreas@silvaco.de

For more information on any of our workshops, please check our web site at ***http://www.silvaco.com***

Hints, Tips and Solutions

Andy Strachan, Applications and Support Manager

Q: How can solution quantities such as Electric Field by saved for plotting against applied bias?

A. There are two types of output files saved by *ATLAS:*

- solution files contain physical quantities mapped to the simulation grid. One solution file is saved per bias point.
- log files which traditionally have saved the terminal characteristics for all bias points.

A new feature of *ATLAS* 4.0 is the addition of a capability to save physical quantities at user-specified locations within the device grid to the log files. A new statement `PROBE` is used to specify the quantity to be saved and the location. For example to save the electron concentration rate at a location [1,0.1] the syntax is:

```
PROBE NAME=my_econc N.CONC \
      X=1.0 Y=0.5
```

The label specified by the `NAME` parameter is used to label the saved quantity in *TonyPlot* and subsequent `EXTRACT` statements.

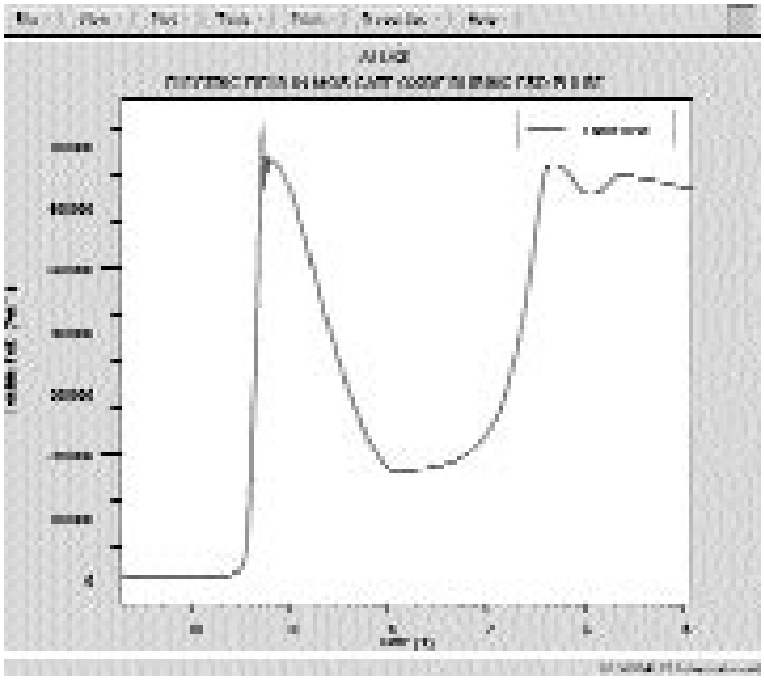

Figure 1. Electric field in MOS gate oxide during a high current pulse on the drain.

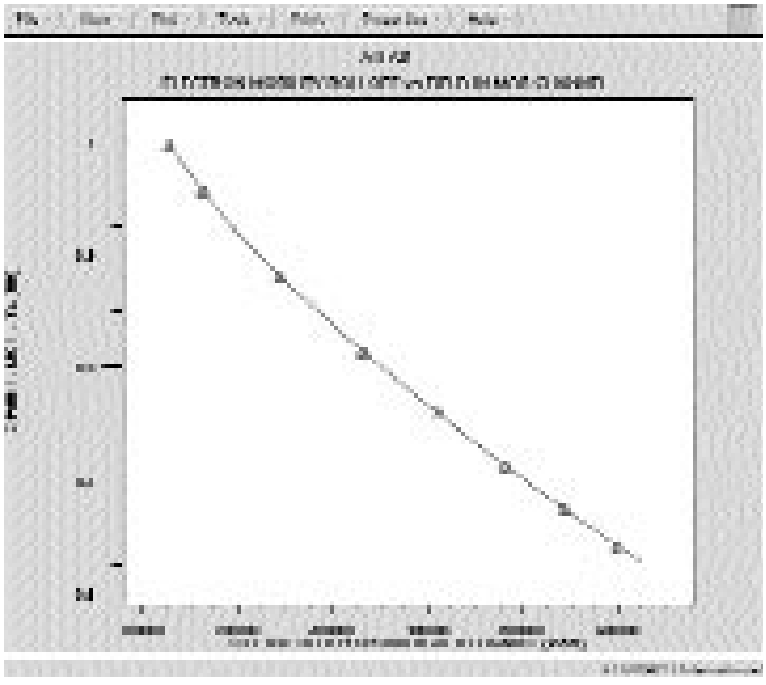

Figure 2. Mobility (normalized) rolls off as a high gate electric field is applied

For vector quantities the `PROBE` statement also requires a direction to be given using the `DIR` parameter. This is specified as an angle in degrees with the X axis as `DIR=0`. To find the electric field across an oxide layer the syntax is:

```
PROBE X=1.2 Y=0.2 FIELD DIR=90 \
      NAME=oxidefield
```

Figure 1 shows the resultant plot of electric field in a MOSFET gate oxide during a transient ESD pulse. This result shows the probability of oxide breakdown during the ESD stress without the need to examine many separate solution files.

Another advantage of the probe for vector quantities is that it reads the values directly from the simulator at the closest location to the specified XY coordinates. This avoids many issues of interpolation and averaging of vector quantities onto the simulation grid.

If two physical quantities are probed at the same location it is possible to plot them against each other to examine model settings. For example, impact ionization rate or mobility versus elec-

tric field. Figure 2 shows a plot of channel electron mobility in a submicron NMOS transistor versus the transverse electric field from the gate.

All of the primary solution quantities can be probed. A full list is given in the manual under the `PROBE` statement. In addition to values at point locations the `PROBE` statement also supports `MIN` and `MAX` parameters to find the minimum and maximum of a given quantity.

Call for Questions

If you have hints, tips, solutions or questions to contribute, please contact our Applications and Support Department

Phone: (408) 567-1000 Fax: (408) 496-6080

e-mail: *support@silvaco.com*

Hints, Tips and Solutions Archive

Check our our Web Page to see more details of this example plus an archive of previous Hints, Tips, and Solutions

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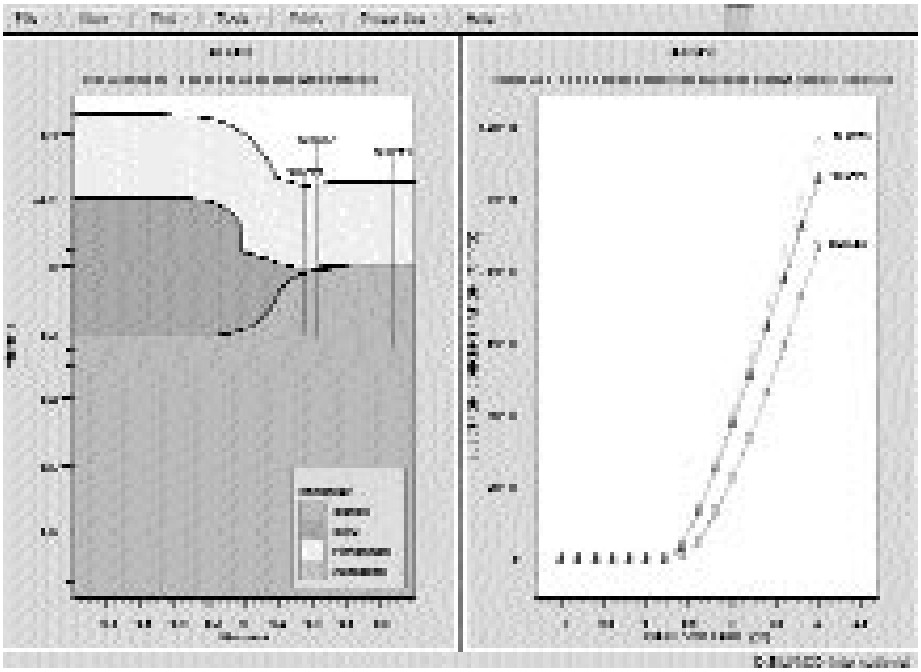

Figure 3. Using a PROBE of electron concentration allows a study of MOS width effect using 2D simulation. An enhanced electron concentration is seen along slice 2.

License Policy Change for TonyPlot™ and DeckBuild™

Starting with the Spring '97 release of ***ATHENA*** and ***ATLAS,*** Silvaco will implement a new licensing policy for the ***TonyPlot*** visualization and ***DeckBuild*** runtime environment ***Interactive Tools***.

The *extensive investment* that has been made by Silvaco in increasing the sophistication of ***TonyPlot*** and ***DeckBuild*** has created a situation in which licensing of these tools must now be better regulated.

For all new purchases, the licensing of ***TonyPlot*** and ***DeckBuild*** as stand-alone will be more rigorously enforced.

In cases where due to development collaboration, exchange of intellectual property rights, or other reasons, additional licenses of ***TonyPlot*** and ***DeckBuild*** were granted, the new licensing policy will exchange all existing licenses according to the following formula:

# of new floating licenses = 2 X # of licensed core tools

The UNIX based core process and device simulators qualified under this program are: ***SSuprem4, SSuprem3, Flash, Optolith, Elite, S-Pisces, Blaze, TFT, Quantum, Laser, FRAM, Luminous, Giga*** and ***Device3D***.

PC versions of ***SSuprem3*** or ***ATHENA*** will continue to be shipped with ***DeckBuild-PC*** and ***TonyPlot-PC*** as a single-user node-locked environment.

Silvaco's assertion of its copyright protection for ***TonyPlot*** and ***DeckBuild*** will now require all existing and future users who wish to establish an interface between these products and third-party simulation tools to receive written permission from Silvaco. Commercial organizations and Universities who wish to maintain any current interfaces with TonyPlot and DeckBuild will also need to contact Silvaco to obtain written permission.

Silvaco is committed to maintaining an open environment. Implementing these changes is intended to insure the future quality of our products.

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