

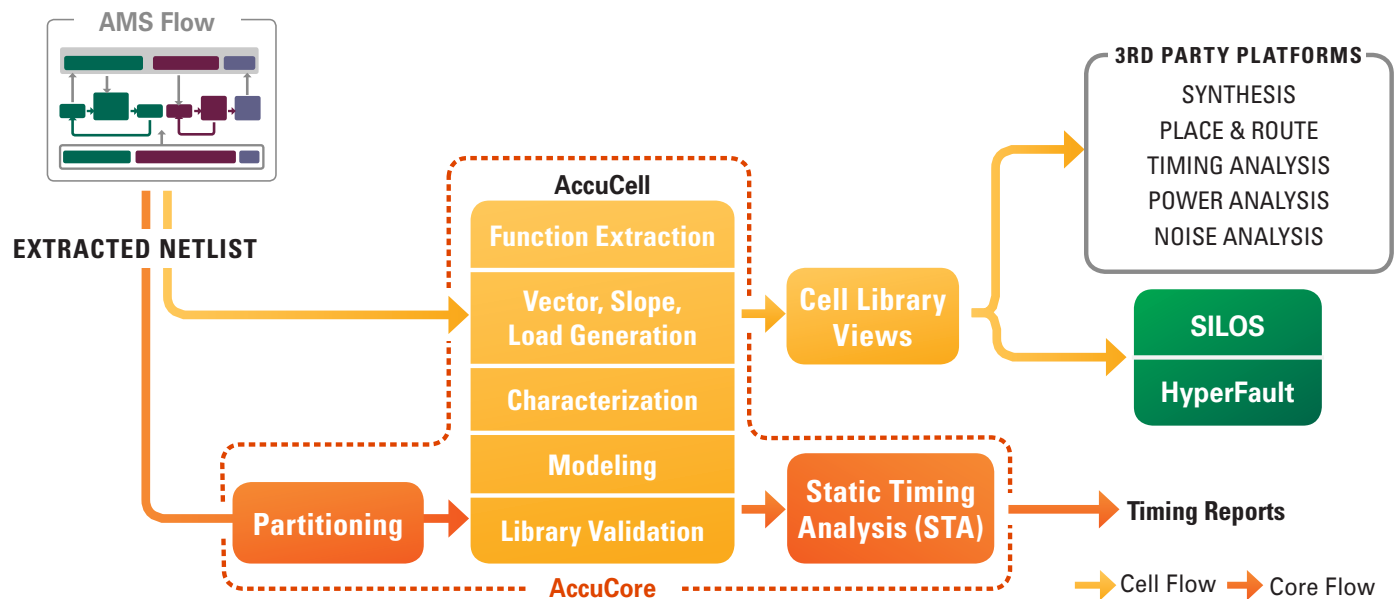
Services for Cell Libraries and Blocks

Services for cell libraries and blocks can provide an excellent way to get the most out of your design flow environment. Services offered include:

- Cell library and block characterization
- COT methodology and setup
- Custom training with your IP

Standard cell libraries, I/Os, custom cells, and cores with accurate timing, power leakage and noise models required by leading synthesis, simulation, optimization, and analysis tools can be provided along with the COT environment to re-create the results.

Characterization and Modeling Process



Cell / Core Characterization Service Deliverables

Synopsys Liberty™ (.lib) – Timing and power file for synthesis, floorplanning, place & route, and static timing analysis tools

Verilog (.v) – IEEE 1364-2001 Verilog models of cells for backannotation and structural verilog netlist (core only)

Cell Documentation – Datasheets with cell configuration, graphic, truth table, timing, power, input capacitance, power consumption, and propagation delays

High Level Timing Models (Core Only) – Black box (complete block or instances of analog circuits embedded in cores) compressed models, and ring models.

Path Reports (Core Only) - all-path timing models, cross reference files, “kept” subcircuits

Customer Cell / Core Characterization Service Deliverables

SPICE Models – HSPICE model files at the foundry supplied process corners (temperature, voltage, process). Silvaco can also extract models from a wafer or measured data and produce a complete measured vs. simulation report for each device.

Extracted Circuit Netlist– SPICE netlists of the cells/cores to be characterized (includes parasitics). If parasitic extraction has not been performed, Silvaco can extract parasitics from GDSII as a service. This option will require customer to deliver extraction and interconnect technology data.

Corners and Options – Customer completes Silvaco Characterization questionnaire to determine characterization configuration including corners, voltages, temperatures, extraction conditions, maximum operating frequency, maximum input transition, input pin capacitance options, setup and hold options, datasheet options, other options, EDA model view requirements and version compatibilities.

Circuit Documentation – In order to verify correct characterization or for unique cells/cores, Silvaco may need access to circuit documentation including schematics, truth-tables, descriptions, and waveforms. Cell schematic graphics files are required if they are to be placed in the datasheets.

SILVACO

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Rev 082610_07