SSuprem4 is a 2D process simulator that is widely used in the semiconductor industry for design, analysis and optimization of various fabrication technologies. SSuprem4 accurately simulates all major process steps in modern technology by using a wide range of physical models for diffusion, ion implantation, oxidation, etching, deposition, silicidation, epitaxy and stress formation. Within the ATHENA framework, SSuprem4 is fully integrated to Optolith for photolithography simulation, Elite for physical etching and deposition simulation and MC Implant for advanced Monte Carlo ion implantation.

Advanced Semiconductor Process Simulation Solutions

• Fast and accurate simulation of all critical process steps used in CMOS, bipolar, optoelectronics and power device technologies

• Simulation of both silicon and advanced semiconductor technologies including SiGe/SiGeC, SiC, GaAs, InP, AlGaAs and InGaAs

• Accurate prediction of geometry, dopant distributions and stresses in device structure allows the elimination or substantial reduction in the number of costly experiments

• Analysis and optimization of standard isolation process LOCOS and modern isolation processes SWAMI, deep and shallow trench isolation

• Analysis and fine tuning of ion implantation processes used at different stages of device fabrication including low energy shallow junction implants, high angle implants for advanced junction formation and high energy implants for deep retrograde well formation

• Hierarchy of impurity diffusion models accurately predict dopant behavior in the bulk and near material surfaces.

• Various diffusion effects are taken into account, including transient enhanced diffusion, oxidation/silicidation enhanced diffusion, transient activation, point defect and cluster formation/recombination, impurity segregation and transport at material interfaces

• Geometrical etch and conformal deposition simulation and analysis of various device geometries

• Seamless interface with lithography simulator Optolith and etching and deposition simulator Elite allows analysis of realistic topology in physical processes

• Automatic interface with ATLAS for subsequent device simulation
Complete Device Fabrication

SSuprem4 is applicable to all silicon IV-IV and III-V device technologies. The comprehensive capabilities of SSuprem4 include robust oxidation models, comprehensive implantation models, a hierarchy of diffusion models and general purpose deposition and etch models, enabling the simulation of complex geometries. Standard MOS and bipolar transistor, devices such as FLASH EEPROM cells, advanced geometry CCDs, HEMTs, HBTs, MESFETs and all types of power devices can be modeled. Any structure created in SSuprem4 can be seamlessly passed to Silvaco’s device simulators for electrical analysis.

ATHENA simulation of a 90nm CMOS process using silicides contacts, halo implants, and shallow junctions.

The figure above illustrates a polysilicon emitter bipolar transistor created in SSuprem4. Accurate base width control is critical to the manufacturing of such devices. The advanced diffusion models in SSuprem4 are able to simulate co-diffusion effects such as emitter push.

Device geometries are larger in power device processing, but the final transistor structures are often two-dimensional in nature. The example shown above is a power DMOS transistor with a self-aligned source contact process.

For advanced CCD structures, lens shaped structures are used to provide increased optical resolution. In the above structure, symmetry is used to speed the simulation time. Only one section of the structure is simulated which is then reflected several times to produce the repeating gate structure used in the electronic device analysis.
The figure above illustrates a buried bit-line EPROM cell. The polysilicon oxidation model allows accurate simulation of important EPROM effects such as the lifting of the polysilicon floating gate and the stress in the inter-poly ONO structure.

The figure above shows simulated GaAs MESFET device structure. The doping in the gate region is formed by low dose 100 keV Be and Si implants while source/drain areas are formed by higher dose 50 keV Si implant with subsequent anneal at 850°C.

This figure shows the pseudomorphic HEMT device. The device is built on the GaAs substrate. The InGaAs channel is sandwiched between two AlGaAs regions. The composition fractions of AlGaAs (0.22 for Al) and InGaAs (0.78 for In) are specified during deposition of the layers. The structure also includes 2 delta dopings above and below the channel which are used as additional carrier suppliers for better control of the threshold voltage. The source and drain regions are made from GaAs and the doping is formed by Se diffusion.
Simulation of 35 minutes boron diffusion at 800°C after ion implantation at 20 keV with a dose of $1.0 \times 10^{14} \text{cm}^{-2}$ (Experiment is from S.Solmi et.al). This simulation and experiment show that even below the solid solubility level substantial portion of dopant remains inactive due to formation of mixed dopant-defect clusters. Due to inclusion of a sophisticated Boron Interstitial Cluster (BIC) model ATHENA accurately predicts this important effect.

Low-Temperature Transient Enhanced Diffusion

Simulation of 10 seconds boron diffusion at 1000 ºC after ion implantation at 2 keV with a dose of $1.0 \times 10^{14} \text{cm}^{-2}$ (Experiment is from B. Colombeau’s doctoral thesis). This type of simulation is extremely difficult because it needs to take into account several competing phenomena including strong defect recombination at the surface and very fast generation and recombination of various pairs and defect clusters. Nonetheless, advanced diffusion models in ATHENA show quite good agreement with experimental profiles.

Advanced Diffusion Simulation

Successful use of low thermal budget processes and ultra-shallow junctions are key manufacturing issues for 90nm and smaller technology nodes. Accurate simulation of low-energy implants with subsequent rapid thermal annealing (RTA) or very low-temperature furnace annealing can be done in SSuprem4 using advanced diffusion models including point defect and defect cluster generation and recombination.

Latching Structure Using MaskViews Interface

SSuprem4/ATHENA interface with Integrated Layout Editor MaskViews allows to simulate complex processes which require specific sequences of mask operation. This interface also automates grid generation as well as specification of electrodes for device simulation.
Oxidation and Silicidation Simulation

Various process steps involve surface reactions and material transformations which result in boundary movements, volume changes and stress formation. SUprem4 simulates two of the most important processes: oxidation and silicidation. Complex local oxidations together with etching and deposition are used to provide advanced isolation structures. Silicides are considered as preferred materials for contact and interconnect metallization.

Deep Trench Isolation

The structure above shows trench oxidation with the interstitials injected by oxidation. Interstitials injected at the oxidizing interface are “trapped” in the trench while those in the silicon diffuse around the bottom of the trench and affect diffusion in the areas to the left of the trench.

Poly-Buffered Isolation

Shown above is an example of poly-buffered LOCOS isolation. The lifting of the polysilicon layer, due to stress, is clearly illustrated.

Stress in Shallow Trench Structure

Stress related reliability and misoperation issues are very important in modern semiconductor technologies. The figure demonstrates stresses built near the corners of a shallow trench during oxidation.

Self-Aligned Silicidation

SUprem4 provides unique capabilities for the simulation of silicide processes. It models the two-dimensional formation of silicides, dopant redistribution and diffusion in the silicide layer. The figure above shows the final structure from a self-aligned silicidation (salicide) process.
Large angle ion implantation is widely used in modern CMOS technology because it allows the optimization of 2D junctions by simply varying ion beam direction. Predictive simulation of large angle implantation is quite challenging because several important effects have to be taken into account. These effects include ion shadowing and backscattering in non-planar structure, considerable channeling along non-vertical crystal channels as well as non-trivial effect of surface oxide thickness on the probability of ions to scatter into those channels. Most of these effects are more pronounced for low-energy (few keV) implants used for shallow junction formation. The Monte Carlo implantation module accurately takes into account all channeling and topological effects. This example shows a 2 keV, 10^{13} cm^{-2} P implant at 45°.

The figure above depicts simulation results using MC Implant and compares them to measured data. The lines are MC Implant simulation profiles; diamonds represent SIMS profiles. Experimental and calculated depth profiles of phosphorus implanted at 100 keV, tilt = 0° and different doses in the range of 10^{13} cm^{-2} to 10^{15} cm^{-2}. Experiments are compiled from R.J. Schreutelkamp et al., “Channeling Implantation of B and P in Silicon”, Nuclear Instruments and Methods, 855, pp. 615–619, 1991.

Aluminium Implants into 6H-SiC

Monte Carlo simulation of Al implants into 6H-SiC at 30, 90, 195, 500 and 1000 keV with doses of 3.0 x 10^{13}, 7.9 x 10^{13}, 3.8 x 10^{14}, 3.0 x 10^{13} ions/cm². The implants were 9° off-axis to avoid channeling. SIMS data are taken from Hernandez-Mangas, et.al. Journal of Applied Physics, v.91, pp.658–667, 2002.

Effect of Oxide Thickness on Boron Implant Profiles

The figure above compares 35 keV, 1.0 x 10^{13} ions/cm², on-axis boron implantation performed through different thicknesses of grown oxide. These simulations use the SIMS-Verified Dual Pearson (SVDP) analytical model based on the tables from the University of Texas at Austin.
Simulation of Well-Proximity Effect

The Well Proximity Effect (WPE), i.e. strong dependence of threshold voltage on transistor location within the well, is caused by an extra non-uniform doping at the surface by high-energy ions scattered within photoresist and emerged from the mask edge at different angles.

![Monte Carlo Ion Trajectories](image)

This figure shows that many of the 2000 boron trajectories simulated by MC Implant Module terminate not in photoresist but at different locations within PWELL. Analysis of these trajectories helps to optimize the thickness and slope of the mask.

![Boron Distribution for Sloped Mask Edge](image)

2D boron implant distribution within PWELL in case of sloped mask edge. Ten million 300 keV boron trajectories were simulated using parallel version of MC Implant Module. Insert shows that boron concentration along the PWELL surface is much lower in the case of sloped mask.

Compound Semiconductor Simulations

All implantation and diffusion models used for silicon technology simulation are available for compound semiconductors. These include analytical and Monte Carlo implant, electric field and point defect effects, segregation and transport at material interfaces. Several specific models are implemented for diffusion in SiGe/SiGeC including the effects of Ge and C content on boron and interstitial diffusivity and intrinsic carrier concentration.

Dopant Codiffusion Effects

![Zinc Diffusion in n-type InP](image)

The figure above demonstrates the effect of n-type doping on Zinc diffusion in InP. It has been found that the main diffusion mechanism for Zn in the III-V compounds is via doubly charged interstitial pairs. Therefore, high background Se (n-type) doping concentration results in a strong retardation of zinc diffusion. Also, the Zn diffusion profiles drop abruptly when n- and p-type concentrations are close to each other near the pn-junction.

Boron Diffusion in SiGe

![Boron Concentration (cm^3)](image)

Comparison of boron profiles for varying initial doping concentrations; structure annealed for 12 hours at 850°C; uniform Ge fraction of 10%. The most outstanding feature of the simulation results is the pileup of boron at the Si/SiGe interface. This occurs because boron has a higher activation energy in silicon than in silicon germanium.
Physical Models and Features

**Diffusion**
- Impurity diffusion fully coupled with point defect diffusion
- Oxidation enhanced/retarded diffusion
- Rapid thermal annealing and Transient Enhanced Diffusion (TED)
- High concentration effects
- TED effects due to implant induced point defects, dopant-defect clusters, and (311) interstitial clusters
- Grain based polysilicon diffusion model
- Transient impurity activation model
- Model which account for Ge and C content on B diffusion in SiGe/SiGeC
- Donor/acceptor co-diffusion effects
- Model for impurity dose loss at silicon/oxide interface

**Implantation**
- Experimentally verified Pearson and dual Pearson implant models
- Non-Gaussian depth-dependent lateral implant distribution functions
- Extended implant moments tables with energy, dose, rotation and oxide thickness variations
- User-defined or Monte Carlo extracted implant moments
- Seamless interface with MC Implant module allows accurate simulation of 2D implant profiles for wide range of energies, doses, field and rotation changes

**Silicidation**
- Models for titanium, tungsten, cobalt, and platinum silicides
- Experimentally verified growth rates
- Reactions and boundary motion on silicide/metal and silicide/polysilicon interfaces
- Accurate material consumption model
- Independent rates for silicon and polysilicon materials

**Oxidation and Stresses**
- Compressive and viscoelastic stress-dependent models
- Separate rate coefficients for silicon and polysilicon materials
- HCL and pressure enhanced oxidation models
- Impurity concentration dependent effects
- Accurate models for simultaneous oxidation and lifting of floating polysilicon regions
- Models for calculation of stresses generated during oxidation or due to thin film intrinsic stress or thermal mismatch

**Deposition, Etching, Epitaxy**
- Extensive geometric etching capabilities including undercut under mask and etch slope angle specifications
- Deposition and etch specification via MaskViews layout editor
- User defined and automatic non-uniform grid specification for deposition and epitaxy
- Uniform and graded multiple impurity doping within deposited layers
- Selective deposition and epitaxy for crystalline silicon and polysilicon

**Structure and Grid Manipulation Features**
- Grid specification via MaskViews interface
- Structure mirroring
- Structure vertical flipping
- Structure stretch
- Relaxation of grid density
- Seamless interface with DevEdit for interactive or automatic structure and grid adaptation
- Direct automatic interface with device simulator ATLAS