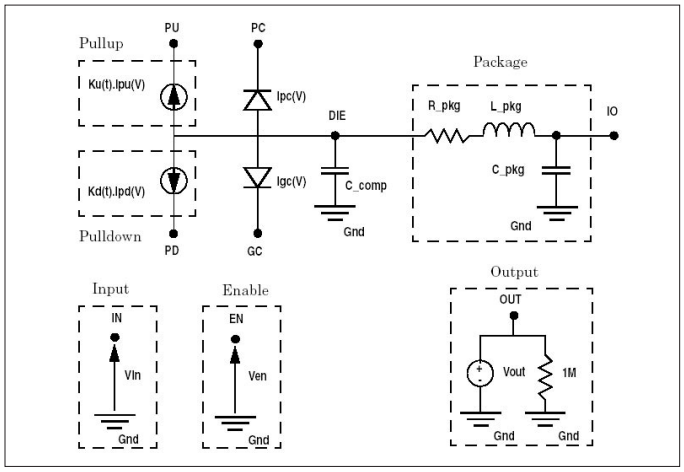
IBIS Support

I/O BUFFER INTERFACE SPECIFICATION

SmartSpice IBIS model support enables semiconductor component vendors to deliver SPICE accurate I/O buffer models for their IC products without disclosing SPICE parameters and transistor netlists. It enables PCB and system designers to accurately simulate high-speed interconnects required for signal integrity when using SmartSpice and semiconductor vendor supplied IBIS models.



General circuit diagram of IBIS devices in SmartSpice.

Key Features

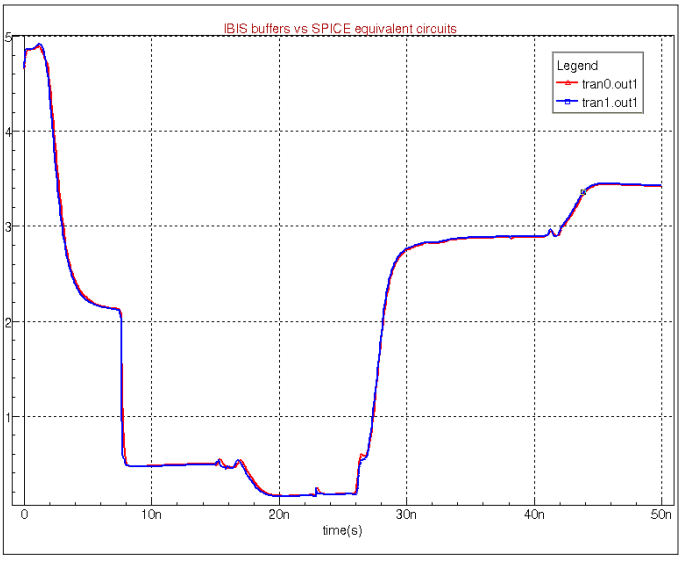
- Enables semiconductor component vendors to deliver SPICE accurate I/O buffer models for their IC products without disclosing SPICE parameters and transistor netlists
- Enables PCB and system designers to accurately simulate high-speed interconnects for signal integrity using SmartSpice and semiconductor vendor supplied IBIS models
- Provides data for typical, minimum and maximum conditions, allowing worst case/best case analysis
- Provides a large amount of information for waveform and timing analysis for system verification
- Silvaco IBIS model support most of the common I/O structures: Input, Input_ECL, I/O, I/O_open_drain, I/O_open_sink, I/O_open_source, I/O_ECL, Output, Open_drain, Open_sink, Open_source, Output_ECL, 3-state, 3-state_ECL and Terminator
- Applicable to most digital components for designing high-speed interfaces (>600 MHz)
- Compatible with IBIS Open Forum specification V4.1 of January 2004

Advantages of IBIS Models as Compared to SPICE Models

- Simulation speed can be 10x – 100x faster than transistor level models (equivalent SPICE circuits)
- Can be as accurate as transistor level models
- Standardization effort of major IC manufacturers and EDA tool vendors allows portability
- Widely available models can be downloaded from manufacturers' web sites (replacement for SPICE models)
- Universally supported with multiple commercial and free software and methodology available for model validation

Compatibility of Silvaco IBIS Model Support

- The latest specification v4.1 released in January 2004 by the IBIS Open Forum is implemented in SmartSpice
- IBIS data is used in their native format (no need for model translation into proprietary modeling formats as implemented in other EDA tools)

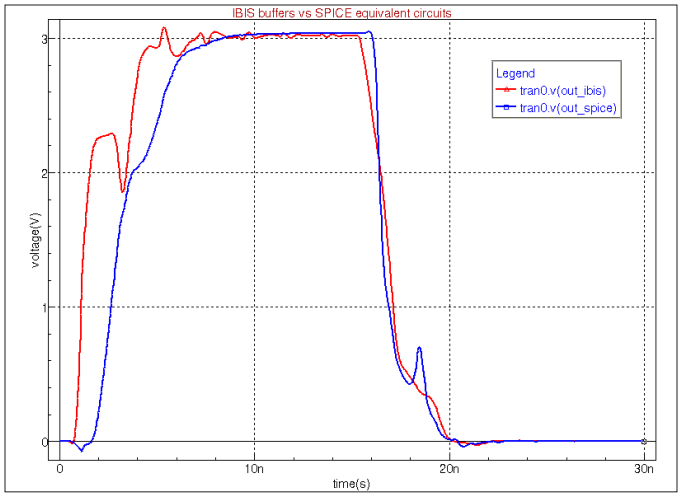


Validation of IBIS models with SPICE results (driver buffer voltages).

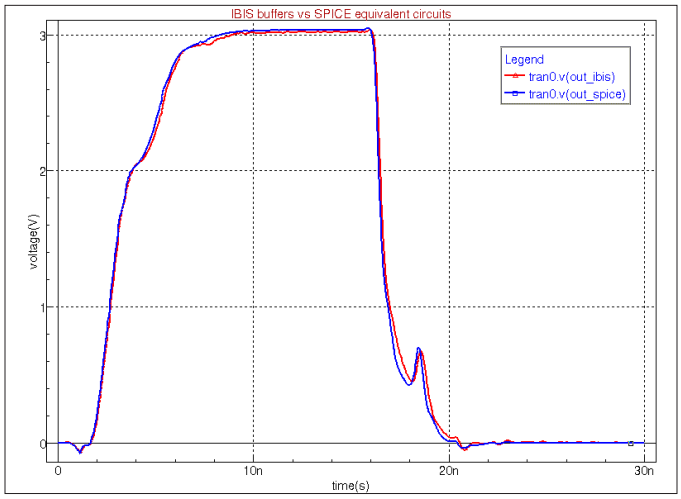
SILVACO

Accuracy of Silvaco IBIS Support

- Supports two-waveform interpolation algorithm to provide the utmost accuracy independent of loading conditions
- Accuracy maintained for overclocked buffers (when the clock period is shorter than the length of V-t curves)
- Mismatch Auto-correction algorithm is implemented to counter balance discrepancies between end points of V-t curves and corresponding operating points derived from I-V curves



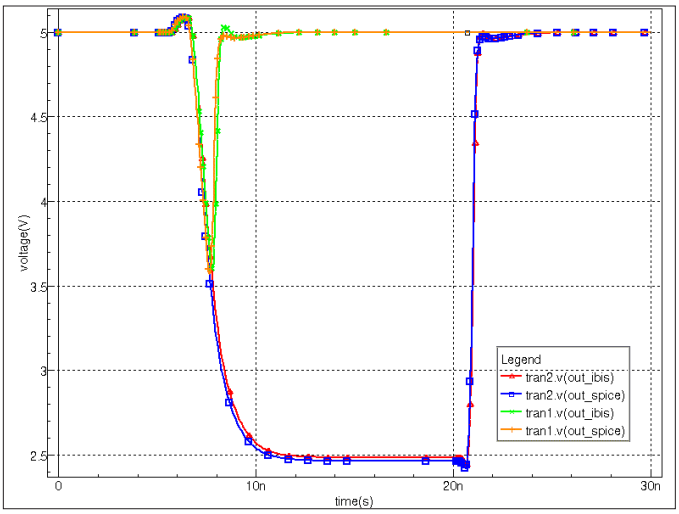
Accuracy loss with one V-t curve interpolation scheme.



Accuracy is maintained with two V-t curve interpolation scheme.

Ease of Use

- Individual buffers and components can be supplied by internal voltage sources or by external voltage sources (or more complex circuits) for SSO simulation
- Extra terminals are available to control or reflect the logical state of the buffer (IN and EN inputs and OUT output)
- Single B-statement may be used to create an individual buffer or a whole component
- Internal variables like multipliers ku(t)/kd(t) and terminal currents can be saved, printed, plotted and /or measured using the standard syntax @Bname[variable_name]
- Further speed improvements are gained through the VZERO option, especially for netlists containing both IBIS buffers and discrete devices (BSIM3v3 transistors for example)



Accuracy of IBIS models maintained for overclocked buffers.

Emerging Standard for Signal Integrity Analysis of Digital Systems

IBIS is a standard (ANSI/EIA-656 and IEC 62 014-1) for electronic behavioral specifications of integrated circuit input/output analog characteristics. It is developed by a committee of EDA vendors, semiconductor manufacturers and end-users, known as the IBIS Open Forum, which is affiliated with the Electronic Industry Alliance (EIA).

IBIS provides formatted data in plain text ASCII files suitable for high-speed designs of digital systems and allows users to evaluate Signal Integrity (SI) and transmission line issues on printed circuit boards (PCB):

- Deformation of electronic signals
- Cross-talk
- Ringing, overshoot, undershoot
- Simultaneous Switching Output (SSO) effect
- Power/ground bounce
- Mismatched impedance
- Line termination analysis
- Reflections
- Topology scheme analysis
- Design rule generation
- Board level simulation

IBIS complete specifications, slide shows, articles, and tools (including Golden Parser executables for most platforms) are available for download at **http://www.eigroup.org/ibis.**

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