Catalyst DA is a software program that translates a structural Verilog netlist into equivalent SPICE format netlist to be used for layout verification or SPICE simulation.

- An automated solution for generating SPICE netlists from Verilog structural description
- Accepts IEEE 1364-2001 Verilog input files
- Capable of generating netlists in Calibre extended SPICE format as well as standard SPICE format
- Performs syntax and syntactical checking of Verilog source files
- Performs a partial translation of Verilog netlists even if some module definitions are not available
- Automatically creates and connects SPICE power and ground nets
- Capable of handling multi-million gate Verilog netlists
- Catalyst DA and Guardian LVS together deliver a complete layout verification solution
- Silvaco’s strong encryption is available to protect valuable customer and third party intellectual property
• Command options can be integrated into an option file for easy reuse and better project management
• Flexible power and ground net naming options
• Option to name primitive gates to resolve name conflicts
• User can add additional pins to a subcircuit definition

Input Example:
```
module top ();
supply1 PWR;
supply0 GND;
wire [0:1] w1;
wire a,b,c;
A inst1 ( 2'b10, w1 );
and inst2 (a, b, c);
endmodule
```

```
module A ( in1, out1 );
input [0:1] in1;
output [0:1] out1;
endmodule
```

Output Example:
```
.subckt top
Xinst1  PWR GND w1[0] w1[1] A
Xinst2  a b c and
.ends

.global GND
.global PWR

.subckt A  in1[0] in1[1] out1[0] out1[1]
.ends
```

Catalyst DA Inputs/Outputs