

# Spider

## Place and Route Design Flow



Spider is a netlist-to-GDSII place and route design flow for mainstream physical design and implementation.

- **Physical Design Flow with n-layer design capabilities ensures the expandability and flexibility needed to meet your tapeout requirements**
- **Advanced Capabilities enabled by the direct database system permits unrestricted “on-the-fly” review and editing of design data and parameters without requiring time-consuming data import and export format translation**
- **Automatic Synthesis of buffers and inverters to aid timing convergence and integrates with external third-party tools and legacy data**
- **Floorplanning with Mixed-Signal Support within the toolset includes automatic placement and “what-if” analysis giving designers an early assessment of timing and area and providing predictable design closure**
- **Placement Optimization features like its automatic net-length minimization and timing-driven algorithms optimize cell placement**
- **Automated CTS features of Spider enable Clock Tree (CT) and High Fanout Net (HFN) Synthesis**
- **Deep Sub-Micron (DSM) Timing-Driven Routing on cost effective server farms**
- **RC and Timing Extraction incorporating both embedded SPICE and RC extraction engines eliminating the need for external tools**

**SILVACO**

## Physical Design Flow

- Physical layout with n-layer design capabilities
- User definable parameters with layout generation coding features
- Supports gate-array, structured-ASIC and standard-cell SoC design styles
- Facilitates control of every aspect of design process
- Highlight nets for review with ease

## Advanced Capabilities and RC and Timing Extraction

- Direct database system permits unrestricted review and editing of design data, and parameters avoiding time-consuming import and export
- Self-Checking Correct-by-Construction Methodology, and warns of potential problems without external checking
- GUI and command-line interfaces with “replay” scripting for run-time automation
- Embedded SPICE and RC extraction engines

## Synthesis Support

- Automatic synthesis of buffers and inverters to aid timing convergence
- Integrates with external third-party logic and physical synthesis tools through timing-driven verilog and DEF based flows
- Imports verilog netlists, SDC/SDF timing constraints and Liberty .lib timing models
- LEF/DEF physical and technology library and design exchange format support

## Floorplanning

- Automatic placement and “what-if” analysis with multiple physical cell-types
- Real-time netlist enforced layout and ECO processes assure error free connectivity control with on-line independent verification and correction utilities
- Built-in netlist, constraint, library and database checking and correction utilities assure valid place and route starting conditions and updates
- Logical hierarchy netlist management with automatic design partitioning and region controlled floorplanning
- Padframe generation with chip and macro power planning and generation
- Automatic utilization estimation and aspect ratio control
- Placement and routing obstruction control features including rectilinear support
- Displayed weighted flylines during floorplanning allow you to place blocks to correctly minimize congestion

## Placement Optimization

- Automatic net-length minimization and timing-driven algorithms optimize cell placement
- 2D congestion map of placement
- Size and/or instance controlled clustering
- Programmable placement strategies permit mixed free-form and datapath-like cell placement methods

## Automated CTS

- Enables Clock Tree (CT) and High Fanout Net (HFN) Synthesis
- Automatically optimizes insertion delay, skew and, inter-clock skew
- Provides delay, transition, skew and, load net details

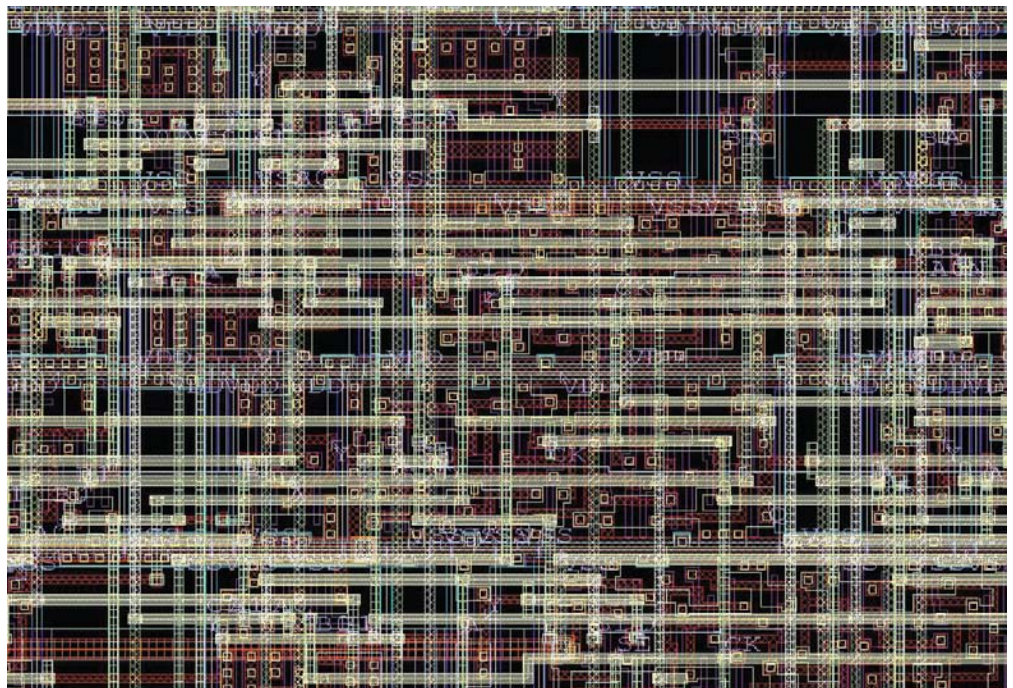
## Routing

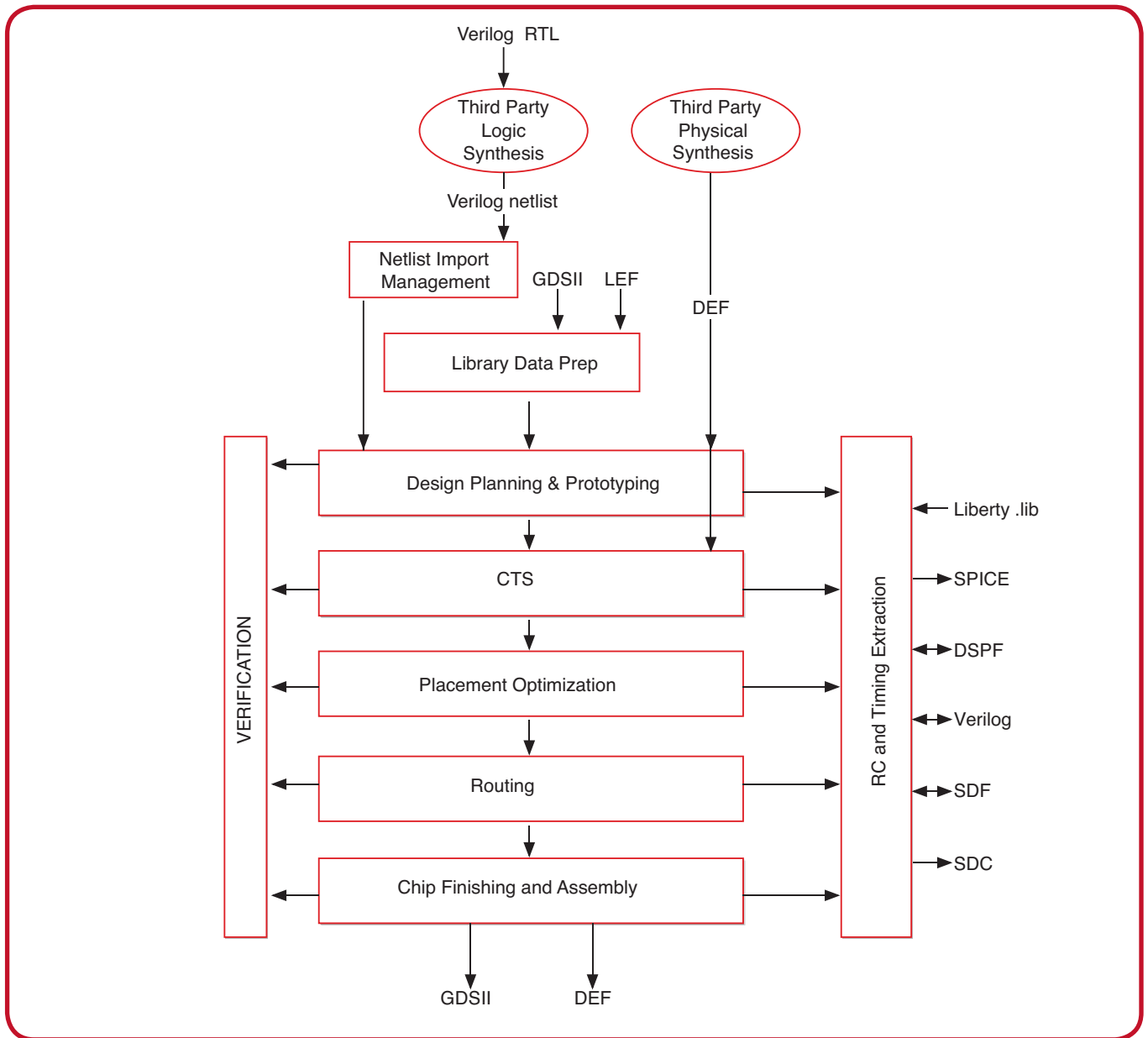
- Performs automatic standard cell and padframe routing
- Timing-driven routing support from SDF forward-annotation and Synopsys™ net timing control files
- Deep Sub-Micron (DSM) design rules support
- Real-time design rule enforced layout and ECO processes assure error free geometry design with on-line independent verification and correction utilities
- Mark specific nets for advanced automatic rip-up and re-route without needing to completely re-run placement and/or routing on the entire design or area
- Programmable automated contour, embedded block, ring, strap, and rail routers make power and ground design and editing a breeze
- Easily perform interactive editing of either power and ground or signal nets with advanced placement and routing editors
- Snap, select, split, move, add corners and change layers during routing simply, and quickly

## Easy to Use Solution

- Easy “what-if” floorplanning analysis capabilities and automatic layout generators
- Powerful UPI and scripting lets you create macros and advanced custom automation environments plus macro automation to simplify repetitive tasks
- Easily replace cells and update the netlist at any time in the design flow
- Simplified top-level assembly and planning with object snapping (gravity)

A screen shot of a routed example.





### Spider Place and Route Design Flow

**Interfaces** –script, macros and GUI

**Inputs/Outputs** –GDSII, EDIF, verilog, LEF, DEF, Liberty .lib, SPICE, DSPF, SDF, SDC

# SILVACO

## HEADQUARTERS

4701 Patrick Henry Drive, Bldg. 2

Santa Clara, CA 95054 USA

Phone: 408-567-1000

Fax: 408-496-6080

## CALIFORNIA

sales@silvaco.com

408-567-1000

## MASSACHUSETTS

masales@silvaco.com

978-323-7901

## TEXAS

txsales@silvaco.com

512-418-2929

## JAPAN

jpsales@silvaco.com

## EUROPE

eusales@silvaco.com

## KOREA

krsales@silvaco.com

## TAIWAN

twsales@silvaco.com

## SINGAPORE

sgsales@silvaco.com



[WWW.SILVACO.COM](http://WWW.SILVACO.COM)

Rev 042513\_12