Digital CAD

Product Line Overview

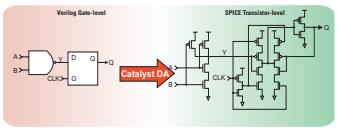
Digital tools for SPICE to Gates, cell library and block characterization, STA, Verilog simulation, and fault analysis.

- **Silos - Verilog Simulator. Easy-to-use IEEE-1364-2001 compliant Verilog simulator. An industry standard since 1986, its debugging features provide a productive design environment for FPGA, PLD, ASIC and custom digital designs.**
- **HyperFault - Mixed-Level Fault Simulator. Verilog IEEE-1364-2001 compliant fault simulator that analyzes test vectors' ability to detect faults. Supports mixed levels of gate, behavioral, and switch with SDF timing.**
- **AccuCell - Cell Characterization and Modeling. Automated, fast and flexible software tool for characterizing and validating standard cell, I/O and custom cell libraries.**
- **AccuCore - Block Characterization, Modeling and STA. Performs timing characterization of multi-million device circuits and performs block and full-chip STA.**
- **Catalyst AD - SPICE Netlist to Verilog Gates Converter. The premier tool for converting transistor-level designs into verilog gate-level representations with applications in microprocessor, DSP, graphics and high-speed communication markets.**
- **Catalyst DA - Verilog Netlist to SPICE Netlist Converter. Translates a structural Verilog netlist into equivalent SPICE format netlist to be used for layout verification or SPICE simulation.**
- **Spider - Place and Route Design Flow. Netlist-to-GDSII place and route design flow for mainstream physical design and implementation.**

SILVACO

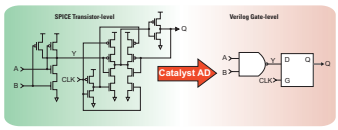
Digital CAD Product Line

Catalyst DA



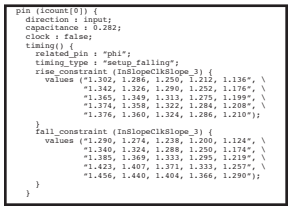
Verilog Netlist to SPICE Netlist Converter

Catalyst AD



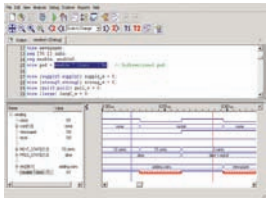
SPICE Netlist to Verilog Gates Converter

AccuCore

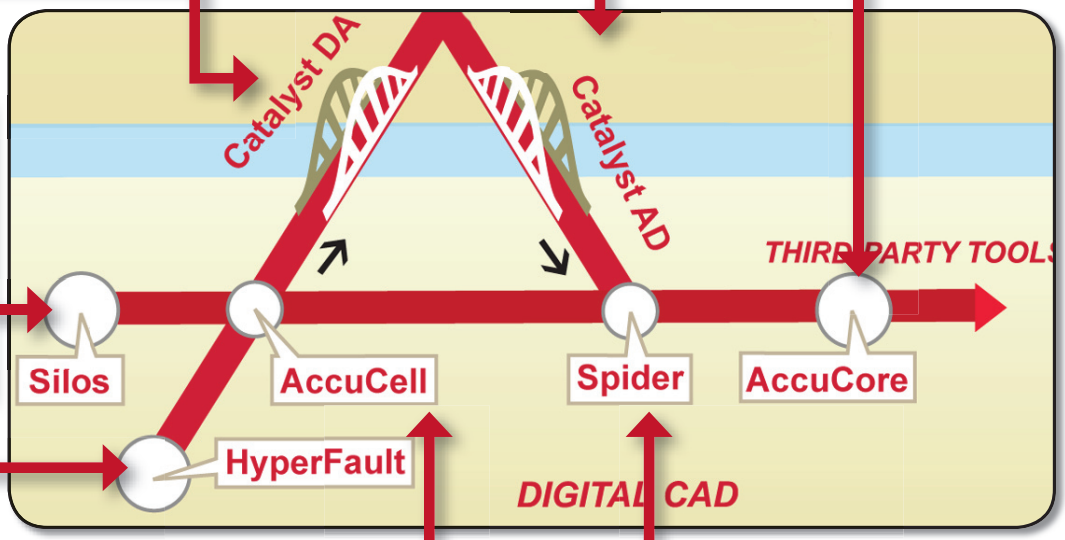


Block Characterization, Modeling and STA

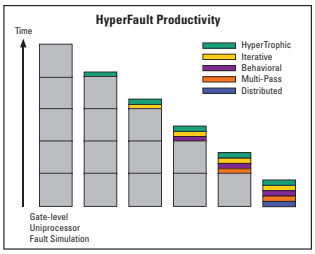
Silos



Verilog Simuator

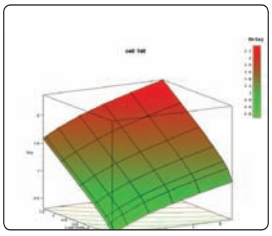


Hyperfault



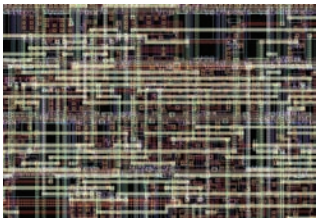
Mixed-Level Fault Simulator

AccuCell



Cell Characterization and Modeling

Spider



Place and Route Design Flow

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