# Custom IC CAD

## Product Line Overview


IC layout, DRC/LVS verification, and RC parasitic extraction environment for analog, mixed-signal and RF design engineers.

- **Expert – Layout Editor. Hierarchical IC layout editor with full editing features, large capacity and fast layout viewing.**
- **Guardian - DRC/LVS/NET Physical Verification. Provides interactive and batch mode verification of analog, mixed signal and RF IC designs.**
- **Hipex - Full-Chip Parasitic Extraction. Performs extraction of parasitic capacitances and resistances from hierarchical layouts.**
- **Clarity RLC - RLC Netlist Reduction Performs reduction of linear parasitic RLC elements in extracted netlists. Based on Scattering-Parameter-Based Macromodeling and Time Domain methods.**

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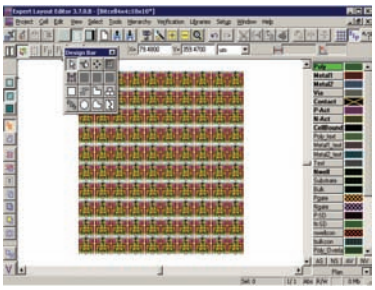
# Custom IC CAD Product Line

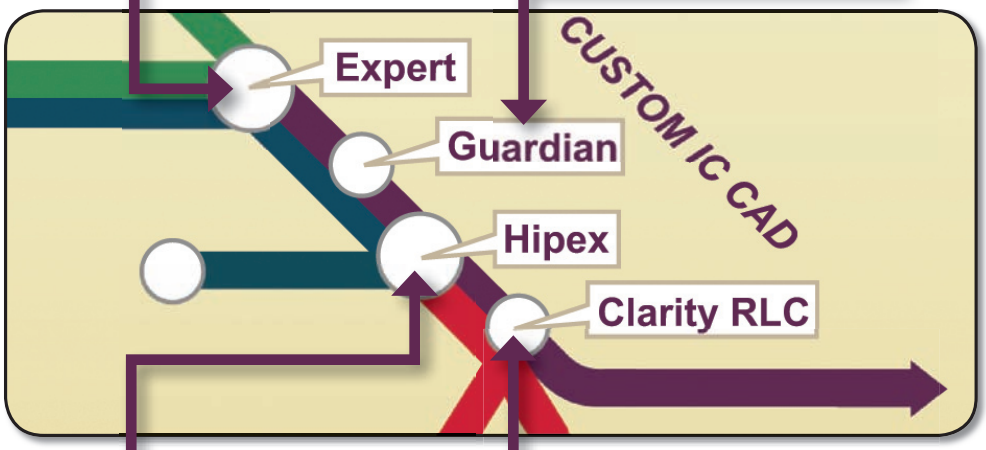
## Expert



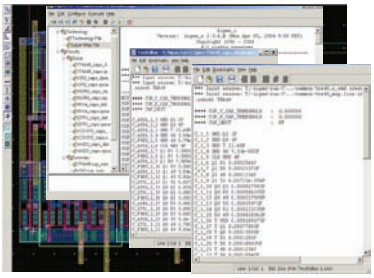
Layout Editor

## Guardian

DRC/LVS/NET Physical Verification

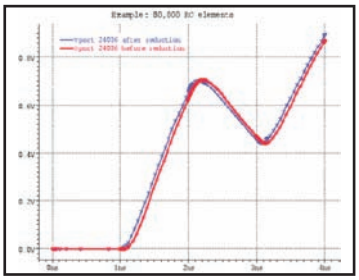



## Hipex



Full-Chip Parasitic Extraction

## Clarity RLC



RLC Netlist Reduction

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