Guardian

DRC/LVS/NET Physical Verification

Guardian provides interactive and batch mode verification of analog, mixed signal and RF IC designs, and is integrated with Silvaco's schematic capture and layout editor. Guardian efficiently performs design rule checks (DRC), layout netlist extraction, and layout vs. schematic (LVS) comparisons.

- **Guardian is optimized for 64-bit Linux architecture**
- **Integration with Expert Layout and Gateway Schematic Editors provides a complete entry-to-verification design flow for analog, mixed-signal and RF designs**
- **Broad support of semiconductor process technologies through foundry-proven process design kits (PDKs)**
- **Fast, intuitive and hierarchical LVS debugging with cross-probing to layout and schematic views**
- **Guardian NET supports stress effects and well proximity parameter extraction**
- **Silvaco's strong encryption is available to protect valuable customer and third party intellectual property**
- **Performs layout vs layout compariasion (LVL)**

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Guardian DRC Key Features:

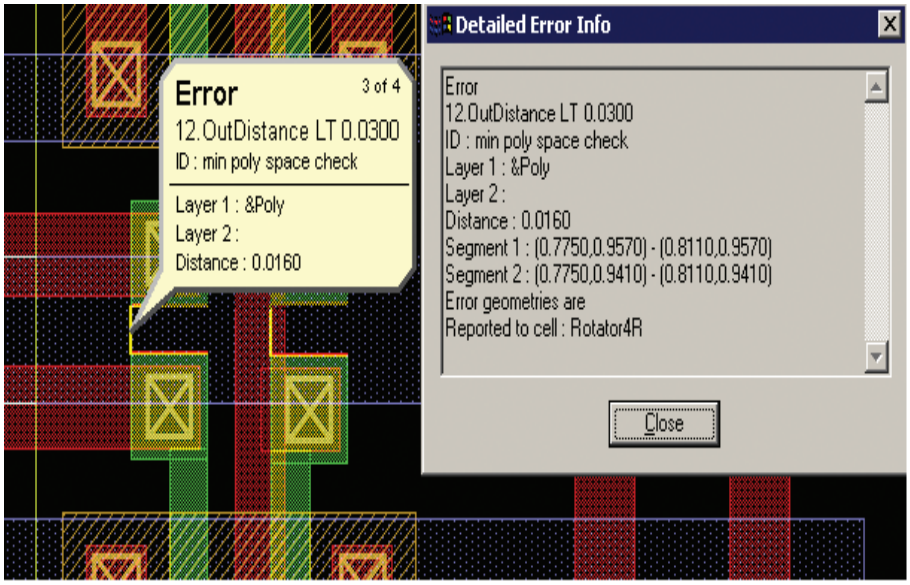
Ease of Use and Adoption

- Compatibility with many leading DRC tools
- Simple installation process does not require consultants to set up environment
- Easy navigation and visualization through graphical and text DRC error reports - intuitive for new users and experts

Productivity and Versatility

- Full DRC command set fits every design environment – local DRC for interactive usage and full-chip DRC in batch mode
- Optimized layer operations based on efficient memory management and advanced algorithms get the most performance from Windows and Linux platforms
- Connectivity-based DRC operations including antenna rule checking
- Optimized execution of DRC commands using graph-based task processing

Productive - Intuitive graphical DRC error debugging in Expert Layout Editor.



Accuracy, Speed, and Capacity

- Supports 90 degree, 45 degree, and all-angle objects with no compromise in accuracy critical for analog and mixed-signal design layout
- Interactive DRC runs within Expert Layout Editor to provide fast DRC of a local area with errors stored in the same error database at chip level to maintain consistency
- Hierarchical DRC report database tracks DRC run history
- Hierarchical DRC error reporting maximizes efficiency of layout debugging
- Multi-threading DRC offers dramatic increase in performance and capacity

Guardian LVS/NET Features:

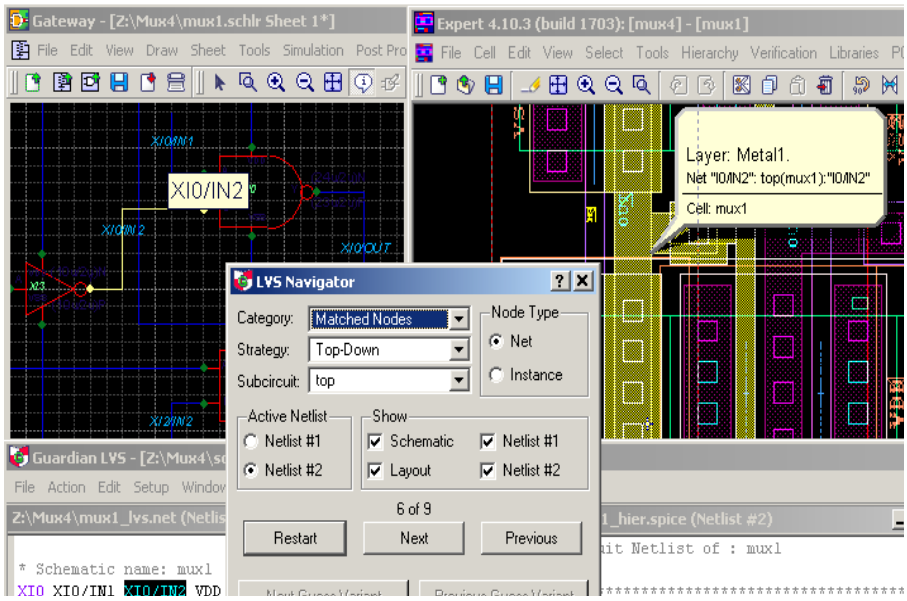
Ease of Use and Adoption

- Intuitive hierarchical LVS discrepancy report significantly decreases time for error debugging
- Direct database links between Gateway Schematic Editor and Expert Layout Editor provides cross-probing as instant graphical discrepancy reports
- Black-box options for subcircuits provides for incremental LVS comparison in hierarchical mode and easy inclusion of IP blocks into the verified design at top level

Accuracy, Speed, and Capacity

- Accurate calculation of geometry-dependent SPICE parameters important for analog design with default or user-defined equations
- Precise identification of generic devices (transistors, diodes, resistors, capacitors, etc.), user-defined devices, and/or black-box subcircuits during LVS trace
- Efficient full-chip layout netlist extraction for any semiconductor process with unmatched performance

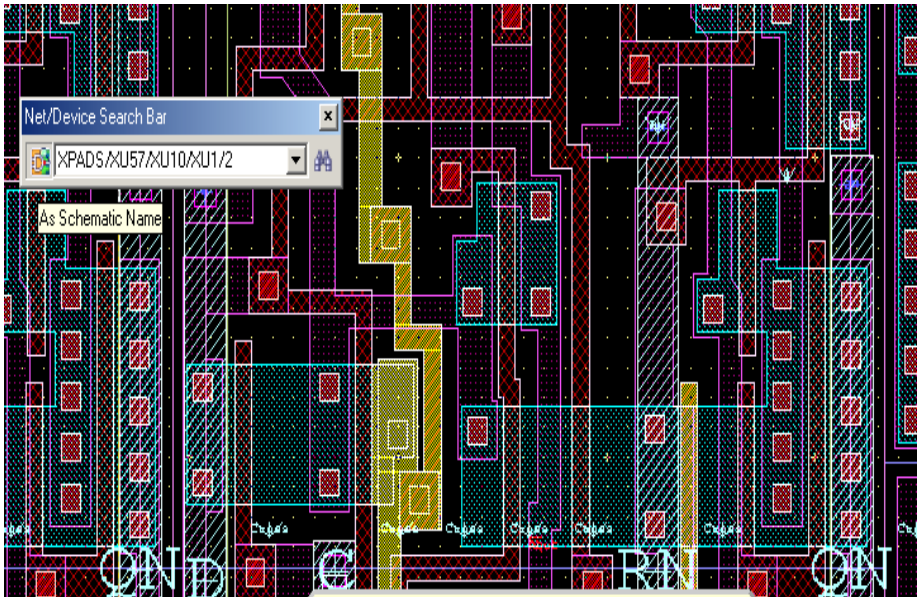
Cross-Probing: Interactive hierarchical cross-probing of LVS discrepancy is clearly displayed.



Productivity and Versatility

- Hierarchical design database supports operations for flat and hierarchical LVS netlist comparison
- Handles any arbitrary shaped polygon geometry used in device formation
- Maximum preservation of original hierarchy for easy debugging during post-layout circuit simulation
- Hierarchical cross-probing of schematic netlist, extracted layout netlist, schematic design, and physical layout
- Detects ERC violations (shorts, opens, dangles, and improperly connected devices) with convenient filtering options
- Supports MOSFET, BJT, JFET, MESFET, diode, resistor, capacitor, and parameterized user-defined devices
- Annotates layout with nodal information enabling such advanced features as Node Probing, Node Search, and Short Locator within Expert IC design environment
- Multi-threading for hierarchical netlist comparison

Node Search highlights nets, devices and instances by schematic and layout names.



Guardian Inputs/Outputs

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