Verilog-A

Verilog-A Language - Source, Compiled and Encrypted

Compiled Verilog-A language combined with SmartSpice provides circuit designers and model developers with an easy-to-use, comprehensive environment for the design and verification of complex analog and mixed-signal circuits and models.

- **SmartSpice Verilog-A is within 2x runtime performance of C-compiled ADMS models**
- **Supports top-down design via behavioral modeling and bottom-up verification of analog and mixed-signal designs**
- **Enables compact model engineers to easily develop proprietary models for any semiconductor technology**
- **Enables executable specification to connect analog and digital engineers in a single design project**
- **Provides secure, transportable method for analog IP distribution and evaluation through encryption full/partial and binary files**
- **A Verilog-A debugger is available under GUI mode of SmartSpice to aid model code development. Verilog-A parameter evaluations are shown enabling user to step through model code**

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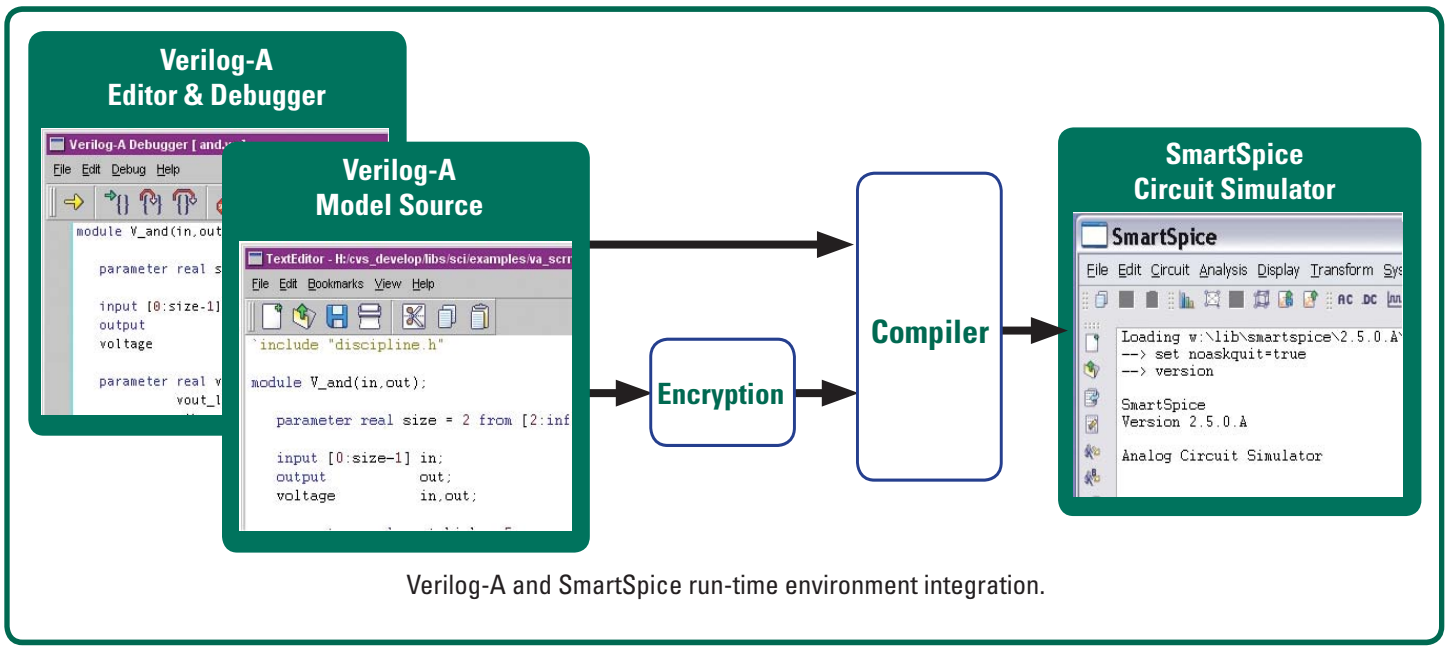
Verilog-A Key Features

- SmartSpice Verilog-A is within 2x runtime performance of C-compiled ADMS models
- Compatible with all analog features of the Verilog-AMS 2.3.1 language specification
- Implements small-signal and noise sources in multiple distributions (Gaussian, exponential, Poisson, chi-square, Student's T, and Erlang)
- Executes analog operators, including time integral/derivative, partial derivative, transition, slew, Laplace transform and Z-transform
- SmartSpice can accept any combination of netlist, C, C++, and Verilog-A for mixed mode execution
- Verilog-A devices can be referenced using the subcircuit X call
- Verilog-A modules can be referenced using the .MODEL statement
- Memory usage and runtime have been significantly reduced by generating a sparse matrix for individual Verilog-A modules
- Support for encrypting or partial encryption of Verilog-A source allows distribution of proprietary models without contents disclosure
- Supports Single Event Upset (SEU) analysis



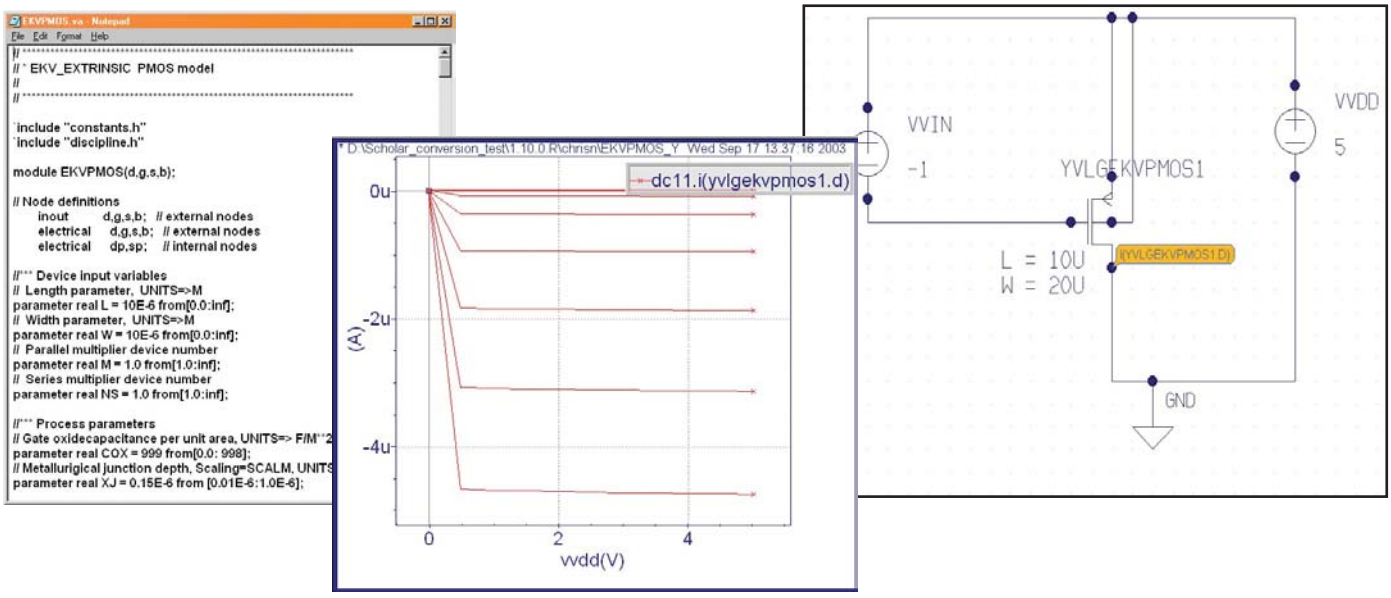
Verilog-A and SmartSpice run-time environment integration.

Analog Behavioral Modeling Environment

- Enables analog designers to build executables for designs of phase-locked loops, VCOs, A/D, D/A, etc. for prototyping purposes before detailed circuit design
- Allows designers to describe digital components as sub-circuits for mixed-signal designs such as Sigma-Delta converters
- Powerful graphical post-processor allows waveform overlays to speed up mixed-signal debugging

Use of SmartSpice Optimizer with Verilog-A

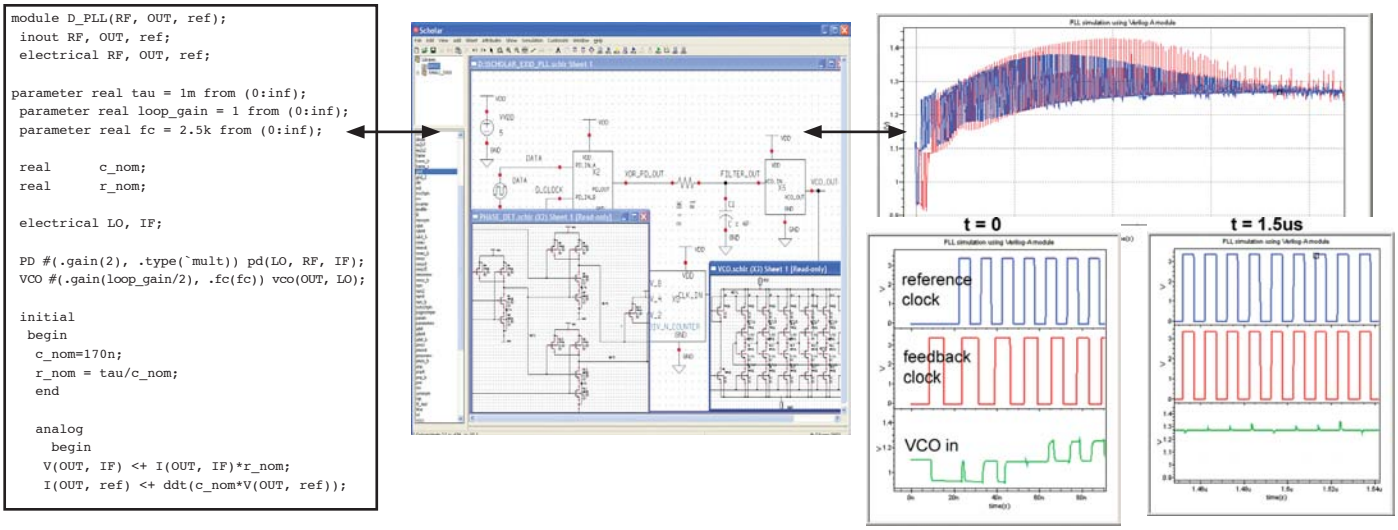
- SmartSpice Optimizer can be used for an input deck which includes Verilog-A module(s)
- Optimization targets can be a combination of:
  - delay, rise time, fall time, and power
  - DC, AC, transient combination of curves
- This can be achieved by optimizing parameters such as:
  - Transistor lengths and widths
  - Device model parameters



Verilog-A environment allows development of compiled models for any .DC, .TRAN, .AC, .NOISE , or .TEMP capability.

Compact Model Development

- Verilog-A compact models are compiled into binary code for rapid execution
- Enables easy development of proprietary SPICE models for specific technologies
- Integrated development and debugging environment accelerates compact model development
- Enables mixing of SPICE model statements and Verilog-A modules in the same SmartSpice netlist



A digital PLL example showing a design flow using Verilog-A.

Verilog-A Inputs/Outputs

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HEADQUARTERS
4701 Patrick Henry Drive, Bldg. 2
Santa Clara, CA 95054 USA
Phone: 408-567-1000
Fax: 408-496-6080

CALIFORNIA	sales@silvaco.com
	408-567-1000
MASSACHUSETTS	masales@silvaco.com
	978-323-7901
TEXAS	txsales@silvaco.com
	512-418-2929

JAPAN	jpsales@silvaco.com
EUROPE	eusales@silvaco.com
KOREA	krsales@silvaco.com
TAIWAN	twsales@silvaco.com
SINGAPORE	sgsales@silvaco.com

WWW.SILVACO.COM

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