HiSIM HV

Surface Potential-Based HV AND LDMOS Compact Model

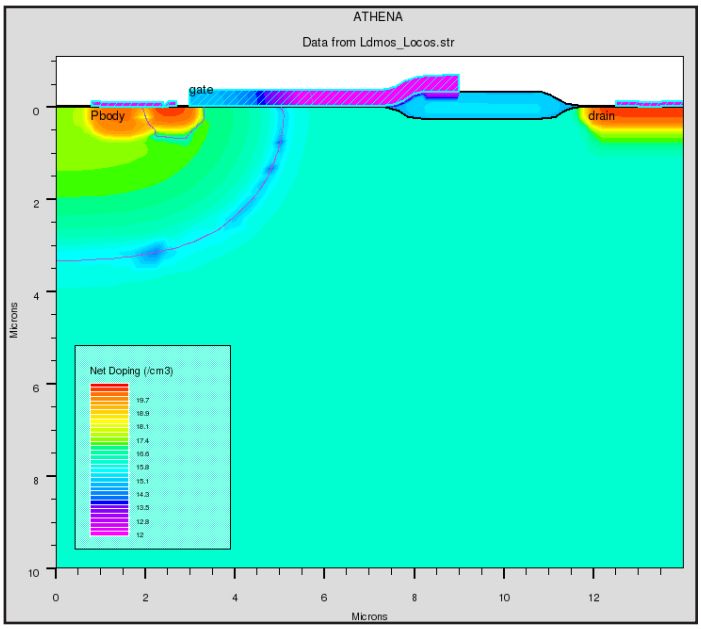
Accurate SPICE Simulation of HV and LDMOS Devices Without Using Macro-Models

HiSIM HV is a surface potential-based model for high-voltage MOSFET devices. The model considers both the symmetrical device structure (HVMOS) and the asymmetrical laterally diffused device structure (LDMOS). All the features of the HiSIM-bulk MOSFET model are preserved in HiSIM HV with extensions mainly to include modeling of the drift region.

Features

The surface potentials along the device surface, including the drift region resistance effects, are calculated iteratively inside the model. This allows a single formulation of model equations to describe the device characteristics and ensures consistent computation of IV and capacitance curves.

- Complete surface-potential-based model
- Considers both symmetrical (HVMOS) and asymmetrical (LDMOS) device structures
- Quasi-saturation effects
- Self-heating effects
- Drift region resistance
- Capacitance including Cgd fall-off
- Impact-ionization effects in the drift region
- Bias-dependent overlap capacitances
- Diode current and capacitances
- Source and drain resistances
- Temperature dependence
- Universal and high-field mobilities
- Channel-length modulation
- 1/f, Thermal and Induced gate noise
- Smooth and continuous derivatives for fast and accurate simulation convergence



Asymmetrical (LDMOS) device cross-section.

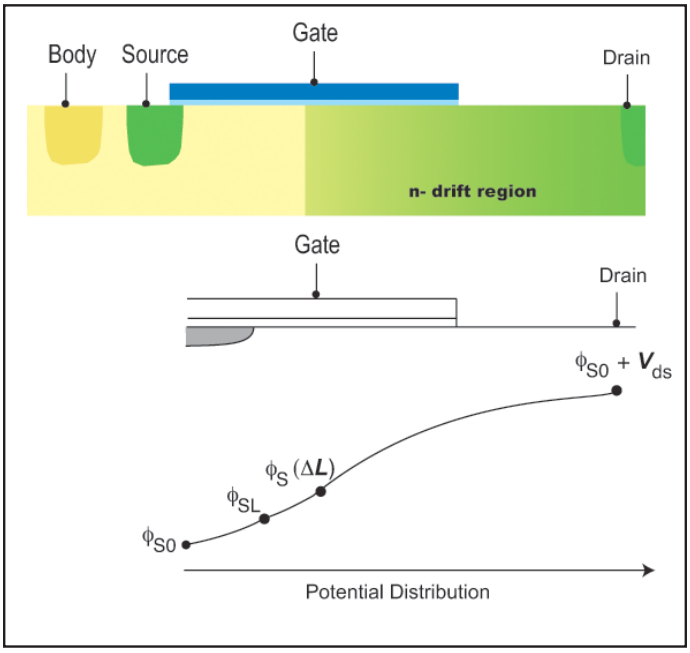
Silvaco Implementation

- The HiSIM_HV 1.2 series is implemented in SmartSpice as LEVEL=73, 172. LEVEL=73 includes Silvaco enhancements for convergence with consistent results with the original university released codes (LEVEL=172). Similarly, the HiSIM_HV 2 series is implemented as LEVEL=75, 173. LEVEL=75 includes Silvaco enhancements and LEVEL=173 uses the original university codes
- All HiSIM HV model implementations are linked to advanced convergence algorithms available in SmartSpice
- Internal warnings and diagnostic provide valuable information to help find convergence issues
- Device internal variables (currents, conductances, capacitances) can easily be accessed like any other model parameter
- HiSIM HV is compatible with BYPASS option in order to achieve great speed performance
- HiSIM HV is compatible with parallel architecture algorithms

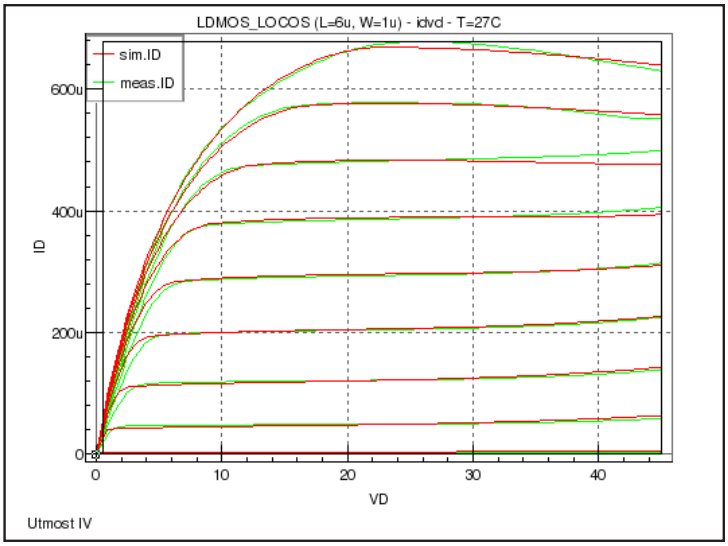
SILVACO

Benefits From Using HiSIM HV

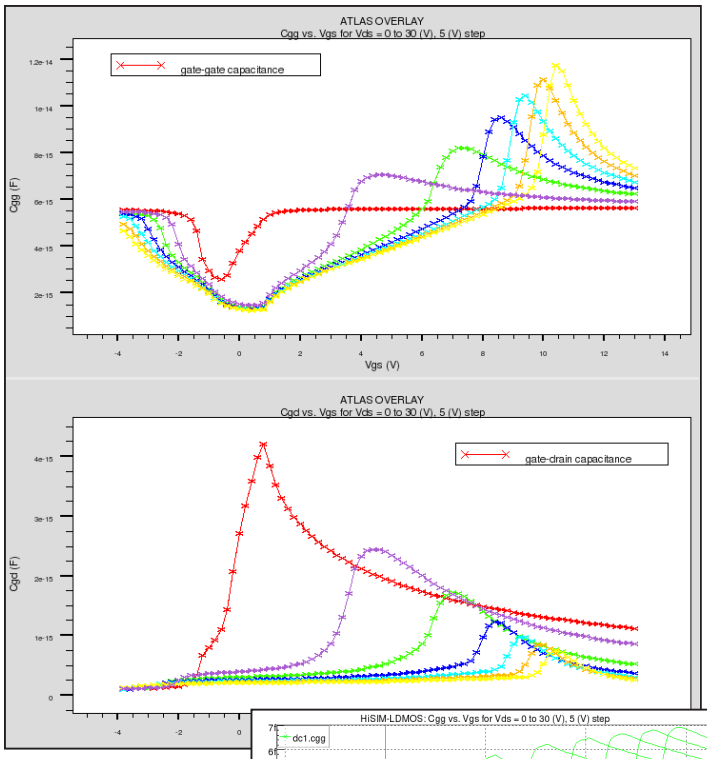
- Single global parameter set – With model scalability, HiSIM HV requires only a single global parameter set for different device geometries. Owing to its surface-potential description, the use of nonphysical parameters is greatly reduced
- Fast simulation time – HiSIM HV enables fast simulation of circuits because it eliminates the use of sub-circuits typical in macro-modeling. The model is stand-alone and instantiated only once for an HV or LDMOS device
- Complete description of HV or LDMOS device characteristics – All principal device model features required by the Compact Modeling Council (CMC) are included in the model. Its surface-potential approach makes it flexible to include variations in HV or LDMOS structure

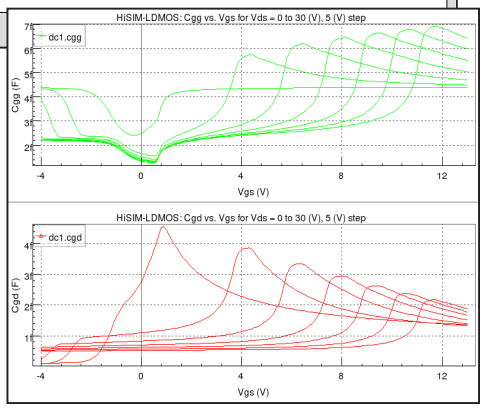


Schematic diagram of HiSIM HV potential distribution for LDMOS case.



Atlas (2D device simulator) and HiSIM HV typical drain current characteristics for LDMOS case. HiSIM HV models the self-heating effect and impact-ionization in the drift region.





Atlas 2D device simulator and HiSIM HV Cgg and Cgd plots for LDMOS case. HiSIM HV predicts the Cgd fall-off.

References

1. HiSIM HV 1.2.2 User's Manual, Copyright 2011, Hiroshima University and STARC
2. M. Yokomichi, et al., "High-Voltage MOSFET Model with Consistently Determined Potential Distribution in MOS Channel and Drift Region," Proc. Int. Workshop on Compact Modeling 2008.