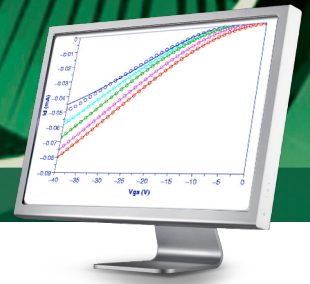


# BSIM4v4

Industry Standard Sub-0.13 Micron MOSFET Model



## Advanced Model Technology for Sub-0.13 Micron and RF High-Speed CMOS Design

Until now, the physical MOSFET device model named BSIM3 version 3.2 and developed at UC Berkeley was considered as the industry standard model for deep sub-micron CMOS circuit design. It was rapidly adopted by IC companies and foundries for accurately modeling devices down to 0.25  $\mu\text{m}$ .

For device scales down to 0.10  $\mu\text{m}$ , some physical mechanisms need to be better characterized. These mechanisms include:

- Velocity overshoot
- Better modeling of weak inversion charges
- Gate bias dependent source and drain series resistance of LDD MOSFETs
- More physical investigation of narrow width effects
- Carrier quantization of MOSFET inversion layers

BSIM4v4 is developed to explicitly address the following issues, for which BSIM3v3.2 was found lacking and inaccurate:

- Accurate modeling of sub-0.13 micron MOSFET devices
- Accuracy in RF, high-frequency analog and high-speed digital CMOS circuit simulation
- Model functionality (geometry-dependent parasitics model)

As a public domain model, BSIM4v4 (like BSIM3v3) is a means of communication, simplifying technology sharing and improving productivity.

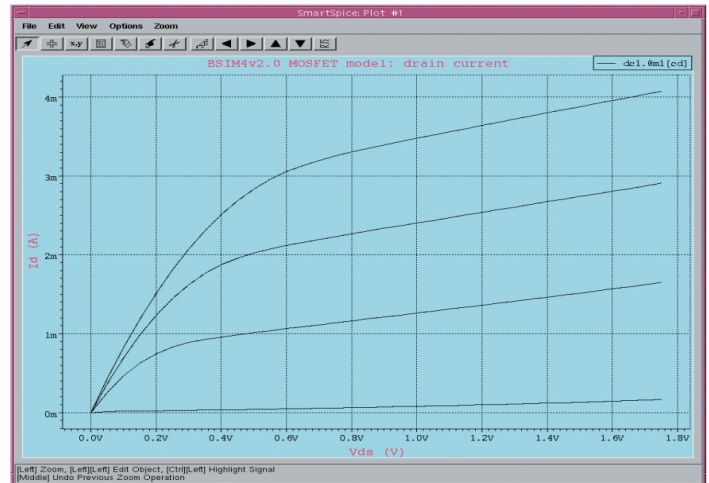
## BSIM4v4 Fundamental Improvements Over BSIM3v3

Like BSIM3v3, BSIM4v4 accounts for major physical effects:

- Short-Narrow channel effects on threshold voltage
- Non-uniform doping effects
- Mobility reduction due to vertical field
- Bulk charge effect
- Carrier velocity saturation
- Drain induced barrier lowering
- Channel length modulation
- Source/Drain parasitic resistances
- Substrate current induced body effect
- Quantum mechanic charge thickness model
- Unified flicker noise model

BSIM4v4 has the following major improvements and additions over BSIM3v3.2:

- Accurate model of the intrinsic input resistance for both RF, high-frequency analog and high-speed digital applications



Main DC characteristics.

- Flexible substrate resistance network for RF modeling
- New accurate channel thermal noise model and noise partition model for the induced gate noise
- Non-quasi-static (NQS) model, consistent with the Rg-based RF model and consistent AC model, accounting for the NQS effect in both transconductances and capacitances
- Accurate gate direct tunneling model
- Comprehensive geometry-dependent parasitics model for various source/drain connections and multi-finger devices
- Improved model for steep vertical retrograde doping profiles
- Better model for pocket-implanted devices in  $V_{th}$ , bulk charge effect, and  $R_{out}$  equations
- Asymmetrical and bias-dependent source/drain resistance, either internal or external to the intrinsic MOSFET
- Acceptance of either the electrical or physical gate
- Oxide thickness as the model input at the user's choice
- Quantum mechanical charge-layer-thickness model for both IV and CV
- More accurate mobility model for predictive modeling
- Gate-induced drain leakage (GIDL) current model, available in BSIM for the first time
- Improved unified flicker (1/f) noise model, smooth over all bias regions and accounting for the bulk charge effect
- Different diode IV and CV characteristics for source and drain junctions
- Junction diode breakdown with or without current limiting
- Gate dielectric constant defined as a model parameter

**SILVACO**

# Overview of Advanced Physics-Based Model Equations

## Basic Current-Voltage (IV) Model

Including:

- A new threshold voltage model for pocket/retrograde technologies
- A  $V_{gsteff}$  formulation, re-derived to achieve better accuracy of gm, gm/Id and gm<sup>2</sup>/Id in the moderate inversion region
- A bulk charge model, with a new formulation of  $A_{bulk}$  to consider its strong effect on doping profile
- Three mobility models, MOBMOD=0 and 1 coming from BSIM3v3.2, and the new MOBMOD=2 corresponding to a universal and more accurate model
- A new output resistance model, especially suitable for long-channel and pocket-implanted devices
- A Gate-Induced-Drain-Leakage (GIDL) current model
- Two bias-dependent  $R_{ds}$  model, corresponding to the BSIM3v3.2 model (internal) or to a new asymmetric model (external), which is more accurate for RF CMOS circuit simulation
- A quantum-mechanical inversion-layer thickness and high-gate dielectrics model, accounted for in both IV and CV
- Trap-assisted tunneling and recombination current model to account for halo-doping technology
- Scalable stress effect model for process induced stress (STI). Device performance varies with active area geometry and location of the device in the active area

## RF and High-Speed Model

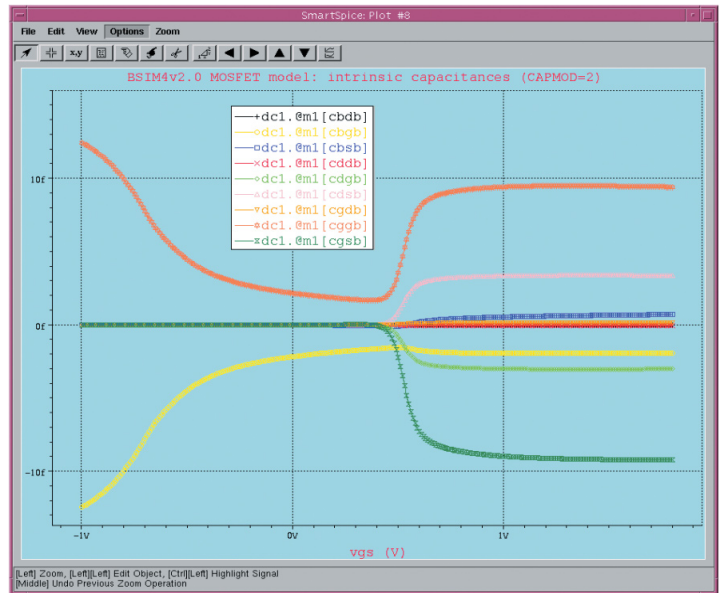
Including:

- Four options for modeling electrode gate (bias-independent) and intrinsic input (bias-dependent) resistances, also working with multi-finger devices (fig.1)
- Two different switches to turn on and off the charge-deficit Non-Quasi-Static (NQS) model in transient and in AC analysis, both AC and transient NQS models based on the same fundamental physics
- A flexible built-in substrate resistance network accounting for the high frequency coupling through the substrate
- A gate dielectric tunneling current model accounting for a current flowing between gate and substrate and a current flowing between gate and channel region, which is partitioned between the source and the drain terminals

## Charge-Voltage (CV) Model

BSIM4 provides three options for selecting intrinsic and overlap/fringing capacitance models, all coming from BSIM3v3.2. The following table maps these models in BSIM4 to those in BSIM3v3.2:

CAPMOD in BSIM4	Matched Intrinsic CAPMOD in BSIM3v3.2.2	Matched Intrinsic Overlap/fringing CAPMOD in BSIM3v3.2.2
0	0	0
1	2	2
2 (default)	3	2



A complete plot of all intrinsic capacitances.

## Parasitics Modeling

- A comprehensive and versatile geometry-dependent parasitics model, providing series and multi-finger device layout modeling capabilities
- Three asymmetrical source/drain junction diode IV models: resistance-free and breakdown-free models coming from BSIM3v3.2 and a new breakdown-and-resistance model

## Noise Modeling

- Flicker noise: a simplified model and a unified physical model are available, both coming from BSIM3v3.2 with several improvements in the unified formulation
- Thermal noise: a long-channel model (coming from BSIM3v3.2) and a new holistic model are available

## Silvaco Implementation

- BSIM4 MOSFET model is part of the ModelLib product-independent model library. It can be accessed within SmartSpice or Utmost III as level 14. Older versions, 0.0, 1.0, 2.0, 2.1 and 3.0, previously released by UC-Berkeley are also supported and are accessible using the model parameter VERSION
- The implementation is fully compatible with the most recent model description issued on March 4, 2004 by UC-Berkeley
- Further speed improvements can be gained through the VZERO option and the multi-threading capabilities
- The diagnostics option EXPERT is supported in BSIM4 to help the designer find convergence problems
- Three selectable STI models : TSMC and Berkeley beta-version models are available in addition to the latest Berkeley model, using the STIMOD selector