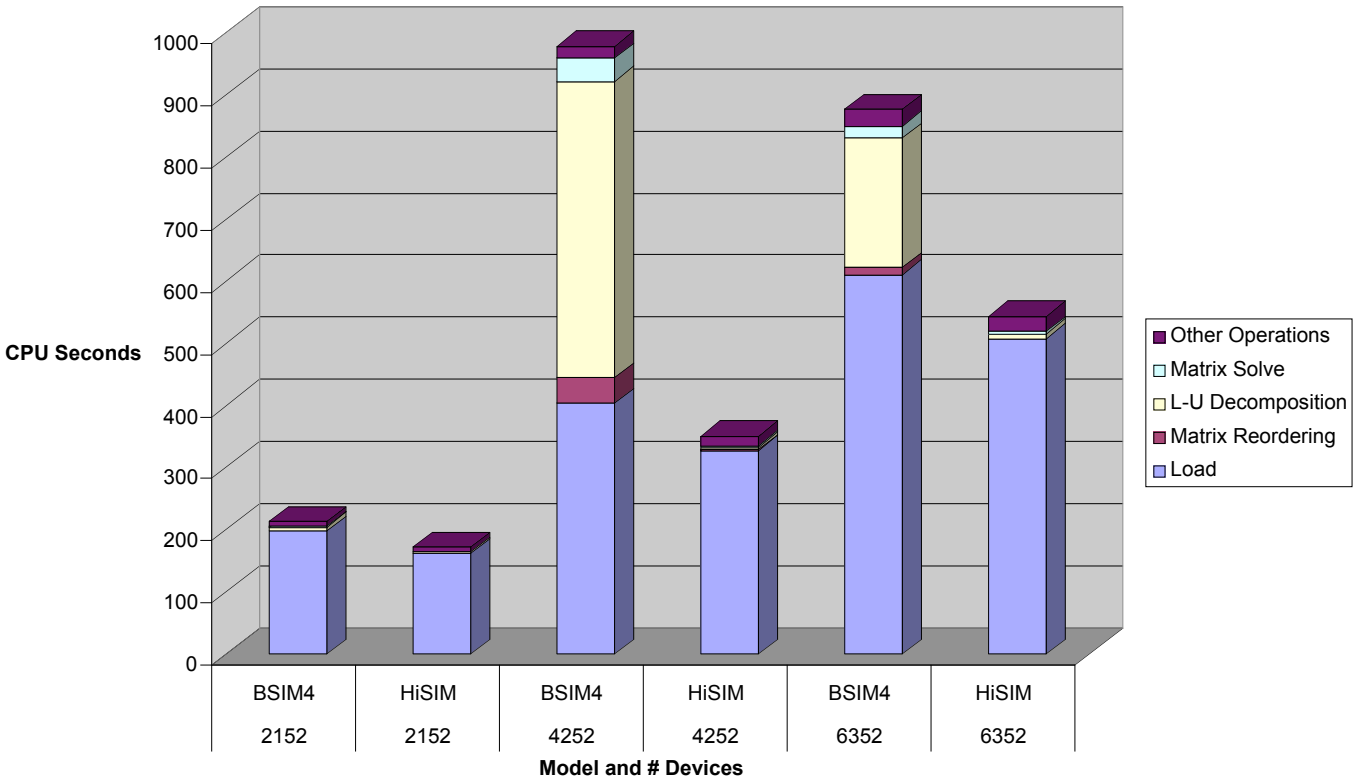
Simulation Speed Comparison Between HiSIM and BSIM4 as Implemented in SmartSpice

Composite graph of 3 sample circuits, details following on next page

BSIM4 vs. HiSIM Performance



Decoder Circuit with SmartSpice Solaris 32

1. Devices#: 2152 – Berkeley Short Channel IGFET Model-4 (level 14, 54) (DEC50)

Computational Statistics of the Transient Analysis

AN.PHASE	time	totiter	totstep	CONrej	DEVrej	MATrej	LTErej	DERrej	breaks
TRAN	204	4345	1970	0	0	0	0	170	244
DCOP	10.1	274	0	0	2				

Description	Time, s	%	Histogram
Total Analyses	214.18		
Load	197.54	92.23	########################
Matrix Reordering	0.36	0.17	#
L-U Decomposition	6.26	2.92	#
Matrix Solve	1.30	0.61	#
Other Operations	8.72	4.07	##

Device	Count	Total, s	Setup, s	Temp, s	Load, s	%	Histogram
BSIM4S	2152	195.84	0.10	0.01	195.73	100.00	#########
Vsource	29	0.00	0.00	0.00	0.00	0.00	

Virtual memory used: 37 617 664

SmartSpice started on Thu Apr 7 15:23:39 2005
SmartSpice finished on Thu Apr 7 15:27:16 2005

1.Devices#: 2152 – HISIM Hiroshima University STARC IGFET Model (level 111):2152 (DEC50)

Computational Statistics of the Transient Analysis

AN.PHASE	time	totiter	totstep	CONrej	DEVrej	MATrej	LTErej	DERrej	breaks
TRAN	170	4089	1867	0	0	0	0	136	244
DCOP	3.01	80	0	0	0				

Description	Time, s	%	Histogram
Total Analyses	172.94		
Load	161.74	93.52	########################
Matrix Reordering	0.09	0.05	#
L-U Decomposition	2.21	1.28	#
Matrix Solve	0.92	0.53	#
Other Operations	7.98	4.61	##

Device	Count	Total, s	Setup, s	Temp, s	Load, s	%	Histogram
HISIM	2152	160.32	0.09	0.01	160.22	100.00	############
Vsource	29	0.00	0.00	0.00	0.00	0.00	

Virtual memory used: 34 783 232

SmartSpice started on Thu Apr 7 15:28:38 2005
SmartSpice finished on Thu Apr 7 15:31:34 2005