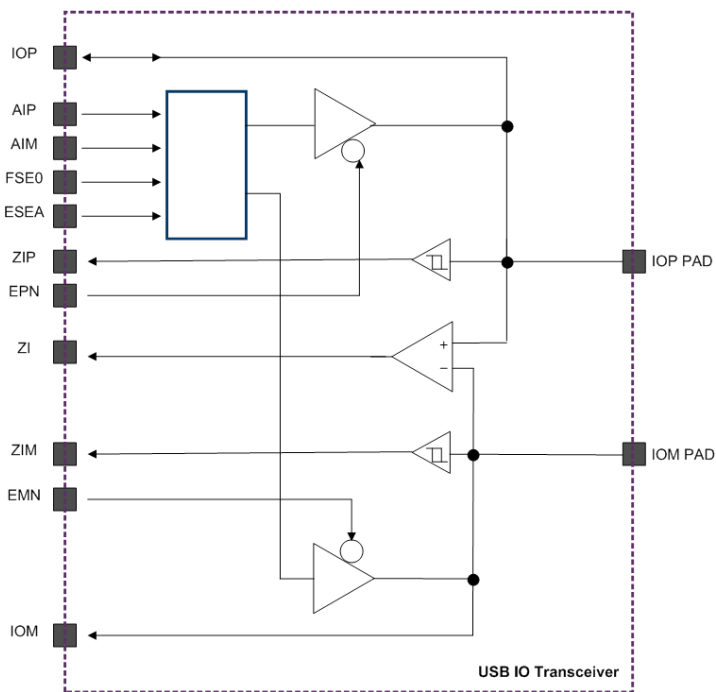


## DESCRIPTION

The USB IO transceiver is a CMOS IO cell available in TSMC 90LP and 65LP processes. It is compliant with the USB specification, Revision 2.0 (Full-Speed and Low-Speed only, April 27, 2000).

The cell transceiver converts logic CMOS signals to USB compatible output signals and vice-versa. The transceiver supports two modes of data transfer rate; Low-Speed mode (1.5 Mbps) and Full-Speed mode (12 Mbps). In both the modes, the amplitude of output signal level is equal to the external supply voltage.

The receiver can detect differential signals as small as 0.2V ( $0.8V < CMR < 2.5V$ ). This gives good noise margin that helps in building a robust communication system. Apart from the differential receiver, the cell also contains two single-ended receivers, one for each of the two data lines.



## FEATURES

- Supports 12-Mbps (Full-Speed) and 1.5-Mbps (Low-Speed) serial data transmission
- Converts logic CMOS signals to USB compatible output signals and vice-versa
- Usable for downstream port of Host, upstream/downstream port of Hub and upstream port of Device
- Individual enable signals for D+ and D- outputs to enable separate control of these two paths for UART mode with same data rates as the USB
- Supports single-ended data interface
- Programmable differential or single-ended core input with forced single-ended low
- IDDQ testable in Suspend mode
- Internal programmable pull-up resistor on D+ data line
- Internal switchable pull-down resistor on both D+ and D- data lines
- No power sequence requirements
- D+ and D- are high-impedance when core is powered down and IO is powered up
- Small area (0.04mm<sup>2</sup> in 90nm)

## DELIVERABLES

- Behavioral model
- Front-end and back-end views
- Documentation including User's Guide and Integration Guide

For more information, please contact us at [ip@silvaco.com](mailto:ip@silvaco.com).

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