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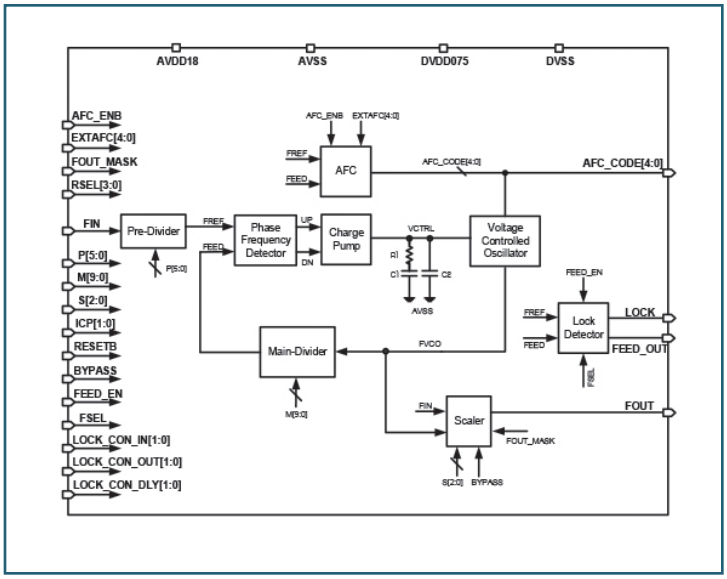
SIPware

2.4GHz Integer PLL

Overview

This is a dual supply voltage integer Phase Locked Loop (PLL). It generates an output clock which is determined by a 6-bit pre-divider, 10-bit main-divider, and 3-bit scaler. The input clock bypass mode, lock detection, and glitch-free function are available.



Key Features

- 8nm low power CMOS device technology
- 1.8V, and 0.85V to 0.75V dual power supply
- Operation junction temperature: -40 to125°C
- Input frequency range: 4MHz to 300MHz
- Output frequency range: 18.75MHz to 2.4GHz
- Period jitter: ±1.5% of VCO clock period
- Output clock duty ratio: 47 to 53%
- Glitch-free post-divider / lock detector / input bypass mode (FOUT=FIN)

Deliverables

- Datasheet
- User guide
- Verilog model
- Timing DK
- CDL netlist
- Layout (GDSII or OAS)

Applications

- Mobile/Consumer/Network

SAMSUNG Foundry

For more information, please contact us at IP@silvaco.com.

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