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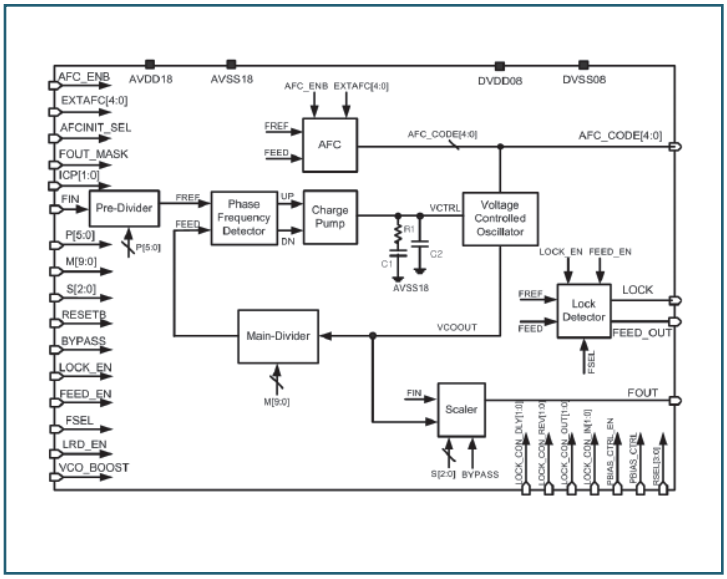
100MHz Low Jitter PLL

Overview

This is a dual supply voltage integer Phase Locked Loop (PLL). It generates an output clock which is determined by a 6-bit input divider, 10-bit feedback divider and 3-bit post-divider. The input clock bypass mode, lock detection and glitch-free function are available.



Key Features

- 14nm Low Power CMOS device technology
- 1.8V, 0.9V to 0.8V dual power supply
- Operation junction temperature (T_J): -40 to 125°C
- Input frequency range: 24MHz/26MHz
- Output frequency range: 100MHz
- Phase Jitter (applying PCIE Standards Masks):
- PCIE Gen1 < 86pspp, PCIE Gen2 < 3.1psrms , PCIE Gen3 < 1.0psrms
- Output clock duty ratio: 48 to 52%
- Glitch-free scaler / Input bypass mode (F_{OUT}=F_{IN})

Deliverables

- Datasheet
- User Guide
- Verilog model
- Timing DK
- CDL netlist
- Layout (GDSII or OAS)

Applications

- Mobile/Consumer

SAMSUNG Foundry

For more information, please contact us at IP@silvaco.com.

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