

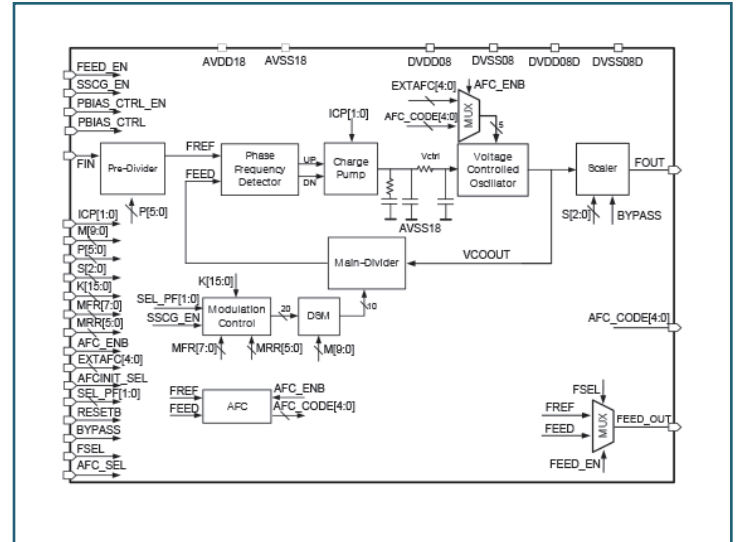
1.2GHz Fractional / SSC PLL

Overview

This is a dual supply voltage fractional and Spread Spectrum Clock (SSC) Phase Locked Loop (PLL). It generates an output clock which is determined by a 6-bit pre-divider, 10-bit main-divider, 3-bit scaler and Delta Sigma Modulator (DSM). The input clock bypass mode, glitch-free function and SSC capability are available.

Key Features

- 14nm Low Power CMOS device technology
- 1.8V, 0.9V to 0.8V dual power supply
- Operation junction temperature (T_j): -40 to 125°C
- Input frequency range: 6MHz to 300MHz
- Output frequency range: 18.75MHz to 1.2GHz
- Period Jitter: $\pm 2.0\%$ of VCO clock period
- Output clock duty ratio: 45 to 55%
- Glitch-free scaler / Input bypass mode ($F_{OUT} = F_{IN}$)
- Spread Spectrum Clock: 20KHz to 150KHz, 0 to 5%, Down/Center/Up spreading



Deliverables

- Datasheet
- User Guide
- Verilog model
- Timing DK
- CDL netlist
- Layout (GDS2 or OAS)

Target Applications

- Mobile/Consumer

SAMSUNG Foundry

For more information, please contact us at IP@silvaco.com.

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