

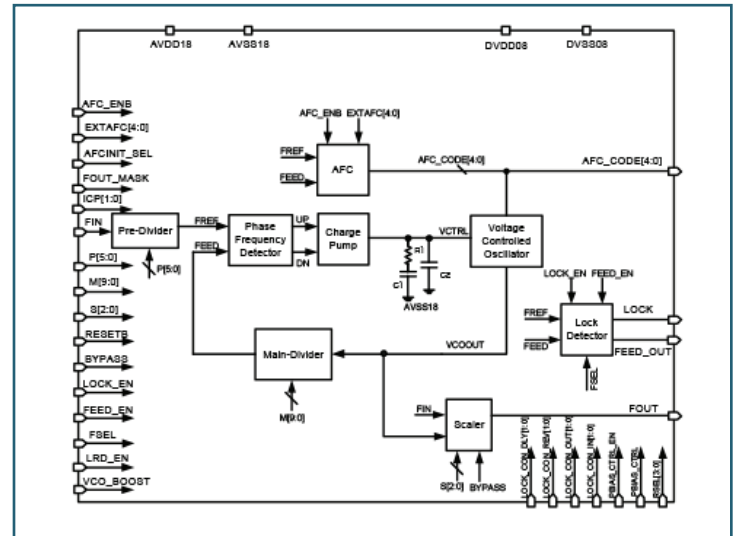
3.2GHz Integer PLL

Overview

This is a dual supply voltage integer Phase Locked Loop(PLL). It generates an output clock which is determined by a 6-bit input divider, 10-bit feedback divider and 3-bit post-divider. The input clock bypass mode, lock detection and glitch-free post-diving function are available.

Key Features

- 14nm Low Power CMOS device technology
- 1.8V, 0.9V to 0.8V dual power supply
- Operation junction temperature: -40 to 125°C
- Input frequency range: 4MHz to 300MHz
- Output frequency range: 25MHz to 3.2GHz
- Period Jitter: $\pm 1.5\%$ of VCO clock period, $F_{VCO} \leq 3\text{GHz}$
 $\pm (0.75\%$ of VCO clock period + 2.5ps), $F_{VCO} > 3\text{GHz}$
- Output clock duty ratio: 48 to 52%
- Glitch-free post-divider / Lock detector/ Input bypass mode ($F_{OUT}=F_{IN}$)



Deliverables

- DataSheet
- User Guide
- Verilog model
- Timing DK
- CDL netlist
- Layout (GDS2 or OAS)

Applications

- Mobile/Consumer

SAMSUNG Foundry

For more information, please contact us at IP@silvaco.com.

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