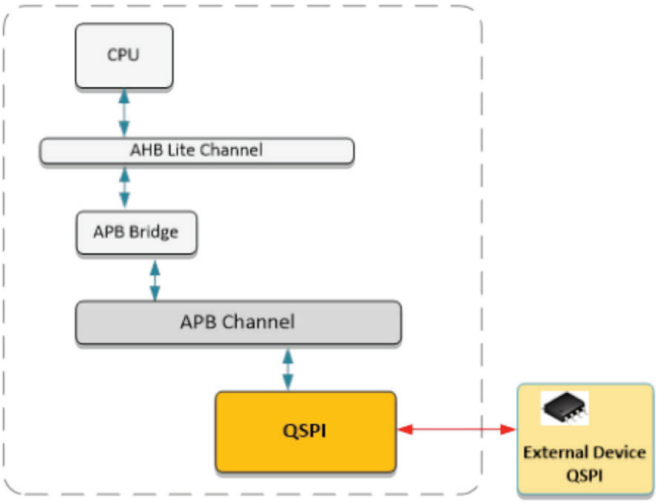
APB Quad SPI Controller

DESCRIPTION

The Quad Serial Peripheral Interface module either controls a serial data link as a master, or reacts to a serial data link as a slave.

The bus controller can be configured under software control to be a master or slave device. Reading and writing the core is done on the AMBA APB bus interface. The core operates in various data modes from 4 bits to 32 bits (8 modes are supported in multiples of 4 data bits). The data is then serialized and then transmitted, either LSB or MSB first, using the standard 4-wire SPI bus interface or the extended Quad mode bus.



FEATURES

- 4 bit to 32 bit serial transmit & receive
- Full and Half duplex support
- Software programmable Master or Slave mode
- Software programmable SCLK rate for Master mode
- Quad-bit mode operation
- Separate SCLK input for Master Mode
- 64 word Tx and Rx FIFOs
- Asynchronous Slave Interface
- AMBA APB interface
- Interrupt control
- LSB or MSB mode
- Up to 4 slaves under Master control
- DMA Interface

FEATURES

- Verilog Source
- Complete Test Environment
- APB Bus Functional Model
- C-Sample Code

For more information, please contact us at ip@silvaco.com.

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