APB Timer IP Core

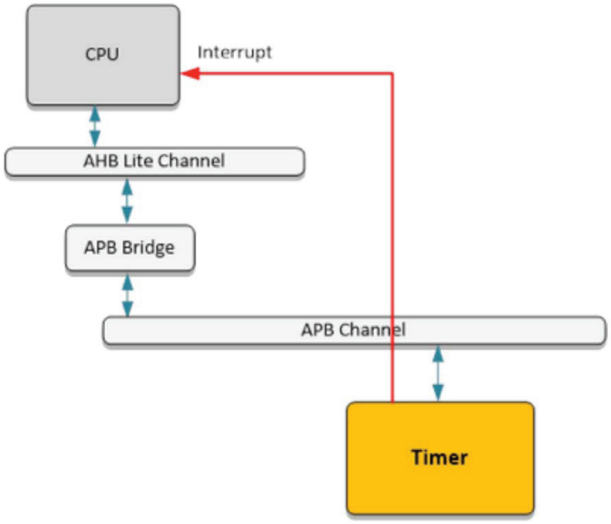
DESCRIPTION

The APB Timer module is a sixteen-bit down counter with a selectable prescaler. Prescale values of 1, 16 and 256 can be selected. The prescaler extends the timer's range at the expense of precision.

The Timer provides two modes of operation that provide a free running value and also periodic interrupts.

The Timer contains several configuration registers that can be written and read by the processor. Two 4-bit prescalers precede a 32-bit counter. The counter can be clocked at either the input clock rate, or a choice of 7 prescaled rates. The counter can be loaded with a value from a preload register. The counter can optionally generate an interrupt.

The Timer module is a standard APB Slave peripheral; the Timer registers are accessed through this interface.



APB TIMER IP CORE FEATURES

- AMBA® APB Compatible
- 16 bit counter/timer
- 10 bit selectable pre-scale
- Periodic and free running event timer modes
- Useful for software or RTOS time base

APB TIMER IP CORE DELIVERABLES

- Verilog Source
- Complete Test Environment
- AHB Bus Functional Model
- C-Sample Code

For more information, please contact us at ip@silvaco.com.

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