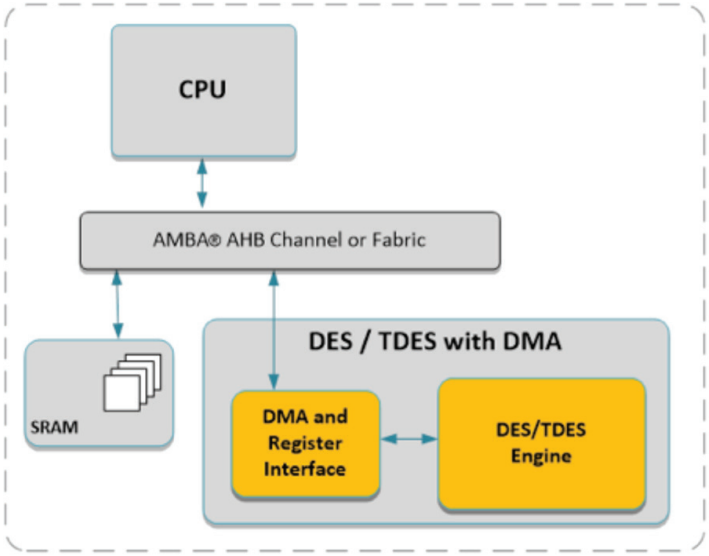
AHB DES and Triple DES with DMA

DESCRIPTION

The AHB DES/TDES Encryption/Decryption Engine is a configurable core that interfaces to an AHB microprocessor bus. The Controller encrypts or decrypts blocks of data based on the DES encryption standard. In order to accommodate a wide variety of system requirements, the Engine can be generated in two modes: LowLatency and LowGateCount. For a TDES system, three DES cores are instantiated. The table below summarizes the options and how to implement them. The checked definitions should be defined and the definitions not checked should be commented out. In this table LL refers to Low Latency and LGC refers to Low Gate Count.



AXI TO APB BUS BRIDGE IP CORE FEATURES

- AHB Master DMA
- AHB Slave Register Interface
- DES/TDES modes supported:
- Electronic Code Book (ECB)
- Cipher Block Chaining (CBC)
- Output Feedback (OF)
- Maskable Interrupt

AHB TRIPLE DES w/ AHB DMA IP CORE DELIVERABLES

- Verilog Source
- Complete Test Environment
- AHB Bus Functional Model
- C-Sample Code

For more information, please contact us at ip@silvaco.com.

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