AHB 4 Channel DMA Controller

DESCRIPTION

The AHB 4 Channel DMA Controller is a multiple-channel direct memory access controller. The DMA IP Core is a Verilog HDL design that can be used in ASIC, Structured ASIC and FPGA designs. The design is intended to be used with AMBA based systems as a controller to transfer data directly from system memory to memory or system memory to peripheral device or IP Core.

Once configured and enabled, the DMA controller is primarily an AHB Master, which initiates data transfers across the AHB bus to/from a peripheral device through the DMA Buffer. The DMA Buffer is a 16x32bit FIFO, which is useful for peripheral devices requiring a steady stream of data such as an LCD Controller, Ethernet MAC or other communication device.

The DMA controller contains useful features such incrementing and non-incrementing addressing and link list operation. Linked list support is useful for non-contiguous memory transfer operations.

The DMA Channel Arbiter determines which DMA Channel has access to the external AHB Master Bus. A round-robin algorithm is implemented in which each active channel has equal priority.

AHB 4 CHANNEL DMA IP CORE FEATURES

- AMBA® AHB Master/Slave DMA Controller
- Four DMA Channels
- Internal Arbitration for Single AHB Master Interface
- Memory to Memory. Memory to Peripheral, Peripheral to Memory, Peripheral to Peripheral modes
- Source and destination address descriptors
- Single word and burst transfer requests
- Programmable burst size
- Current address status
- Incrementing and non-incrementing addressing
- Linked list support
- Transfer complete interrupt AMBA® 2.0 Compatible

AHB 4 CHANNEL DMA IP CORE DELIVERABLES

- Verilog Source
- Complete Test Environment
- AHB Bus Functional Model
- C-Sample Code
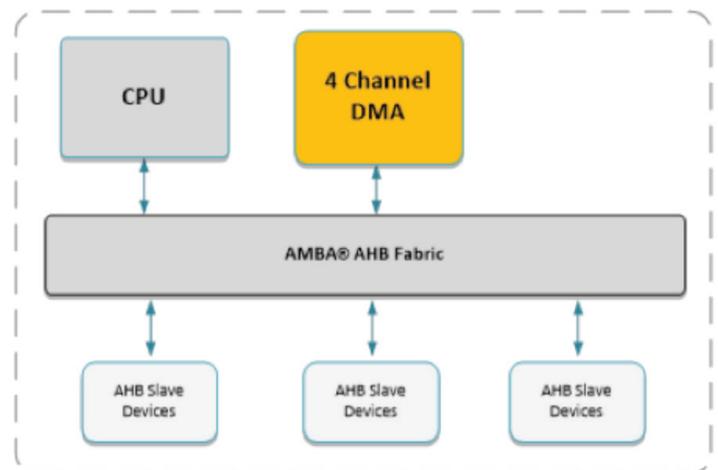
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