

AHB Octal SPI Controller with Execute in Place (XIP)

DESCRIPTION

The Octal Serial Peripheral Interface (OSPI) core is a serial data link (SPI) master which controls an external serial FLASH device.

Reading and writing the core is done on the AMBA® AHB bus interface. The data is then serialized and then transmitted, either LSB or MSB first, using the standard 4-wire SPI bus interface or the extended Dual, Quad or Octal Bus modes.

The OSPI is compatible with various industry-standard DMA controllers. DMA operation in the OSPI can be enabled to assist a DMA controller in the loading (writing) of the transmit FIFO, and the unloading (reading) of the receive FIFO.

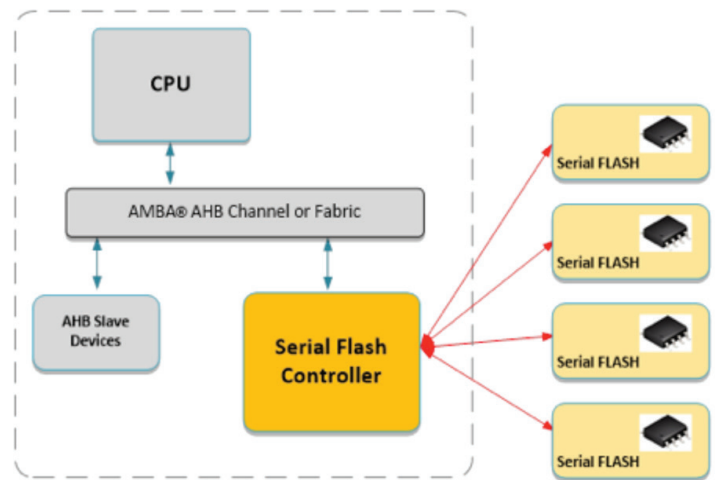
The Execute in Place (XIP) Mode allows an AHB Master to directly read the contents of any of several industry-standard FLASH devices (such as Winbond, Macronix, Spansion and Micron devices) simply by reading from the address space of the QSPI Controller.

OCTAL SPI CONTROLLER IP CORE FEATURES

- 4, 8, 16 or 32-bit serial transmit & receive
- Full duplex operation
- Half duplex operation support
- DTR (Dual transfer rate) support
- Dual, Quad, Octal modes
- Configurable 64 word Transmit FIFO
- Configurable 64 word Receive FIFO
- AMBA AHB interface
- Interrupt control
- LSB or MSB mode
- Up to 4 slaves under Master control
- DMA Interface
- Compatible with most industry-standard FLASH devices
- Execute-in-place (XIP) functionality for several industry-standard FLASH devices

OCTAL SPI CONTROLLER IP CORE DELIVERABLES

- Verilog Source
- Complete Test Environment
- AHB Bus Functional Model
- C-Sample Code



For more information, please contact us at ip@silvaco.com.