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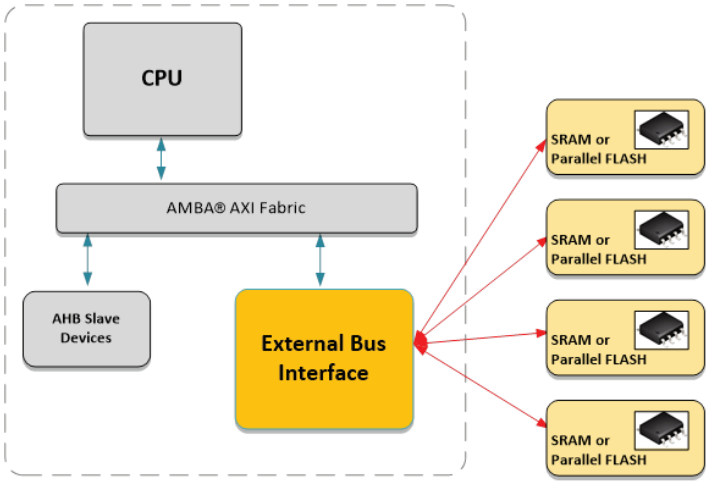
SIPware

AXI External Memory Controller

DESCRIPTION

The AXI External Bus Interface (EBI) allows the processor to transmit and receive data to an external device, usually a memory (SRAM, Flash, etc.). The number of read wait states, the number of write wait states, and the memory width are all configurable through the APB register interface of the EBI. The EBI allows word, half-word, and byte width addressing to 64-bit, 32-bit, 16-bit, and 8-bit external devices.



AXI EXTERNAL BUS INTERFACE IP CORE FEATURES

- Interfaces AXI bus to external SRAM or Parallel Flash devices
- AMBA® AXI Compatible
- Supports 8-bit, 16-bit, 32-bit and 64-bit external modes
- Supports byte (8bit), halfword (16-bit), word (32-bit) and dword (54-bit) internal accesses
- Independent programmable wait states per device interface
- Selects up to 4 external devices

AXI EXTERNAL BUS INTERFACE IP CORE DELIVERABLES

- Verilog Source
- Complete Test Environment
- AXI Bus Functional Model
- C-Sample Code

For more information, please contact us at ip@silvaco.com.

SILVACO

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