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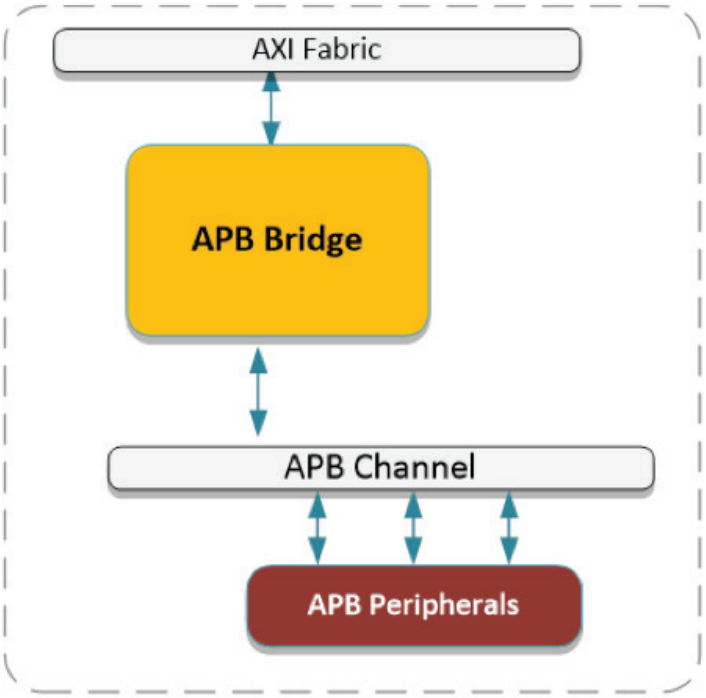
SIPware

AXI to APB Bus Bridge

DESCRIPTION

The AXI to APB Bridge translates an AXI bus transaction (read or write) to an APB bus transaction. This is accomplished via two state machines – one governing the AXI transactions, and one governing APB transactions.

The AXI to APB Bridge acts as an AXI Slave, and an APB Master in an AXI/APB subsystem. Typically, the AXI to APB Bridge has its AXI interface connected to a Slave port on an AXI Channel/Interconnect module, and its APB interface connected to the Master port on an APB Channel module.



AXI TO APB BUS BRIDGE IP CORE FEATURES

- Translates AMBA® AXI transactions to APB transactions
- Low latency
- Low Gate Count
- Supports APB 2.0 and APB 3.0 Signaling
- Independent ACLK, PCLK pseudo-synchronous clocks

AXI TO APB BUS BRIDGE IP CORE DELIVERABLES

- Verilog Source
- Complete Test Environment
- AHB Bus Functional Model
- C-Sample Code

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