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SIPware

# Versatile APB Quad Timer

## DESCRIPTION

The Versatile Timer Unit contains four fully independent 16-bit timer subsystems. Each timer subsystem can operate either in dual 8-bit PWM configuration, as a single 16-bit PWM timer, or as a 16-bit counter with two input capture channels.

Each timer subsystem contains an 8-bit clock prescaler, a 16-bit up-counter, and two 16-bit registers. Each timer subsystem controls two I/O pins that either function as PWM outputs or capture inputs, depending on the associated timer subsystem's mode of operation:

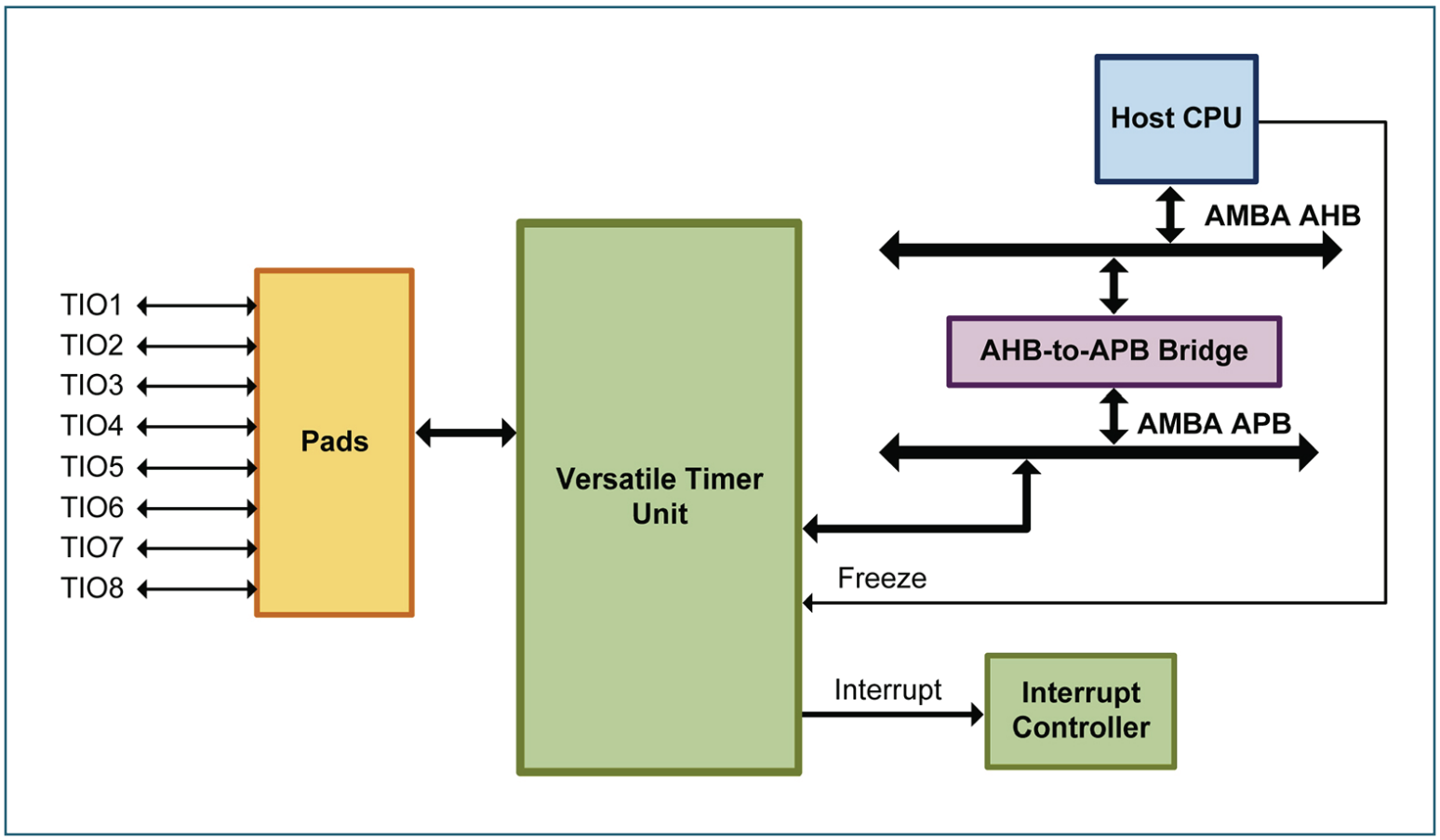
- In 16-bit PWM mode, the TIOx pins function as PWM outputs.
- In dual 8-bit PWM mode, the 16-bit counter functions a two independent 8-bit counters. The TIOx pins function as PWM outputs.
- In capture mode, the TIOx pins function as capture inputs.
- In low-power mode, the clock is stopped. Read operations to the timer subsystem return the current register value; write operations are ignored.

There are four system-level interrupt requests, one for each timer subsystem. Each system-level interrupt request is controlled by four interrupt-pending flags, each of which offers a separate enable/disable bit.

The host interface of the Versatile Timer Unit complies with the AMBA 2 APB protocol. Control registers within the Versatile Timer Unit provide CPU control of timer mode, I/O pin functions and

polarity, clock prescaling, PWM period and duty cycle, enabling/disabling/clearing interrupts, and starting/stopping the counters. Status registers indicate timer/capture values and interrupt status.

There are eight off-chip interface signals, TIO1–TIO8, two for each timer subsystem. To reduce chip-level pin count, the TIO1–TIO8 pins can be shared with other on-chip functions through a General Purpose I/O Controller.



## FEATURES

- Software-configurable to offer up to:
  - Eight fully independent 8-bit PWM channels
  - Four fully independent 16-bit PWM channels
  - Eight 16-bit input capture channels
- Four timer subsystems, each of which contains:
  - One 16-bit counter
  - Two 16-bit capture/compare registers
  - One 8-bit fully programmable clock prescaler
- Each timer subsystem can operate in the following modes:
  - Low-power mode (all clocks are stopped)
  - Dual 8-bit PWM mode
  - 16-bit PWM mode
  - Dual 16-bit input capture mode
- Eight I/O pins, each of which can function either as:
  - PWM output with programmable output polarity, or
  - Capture input with programmable event detection and timer reset
- Flexible interrupt scheme with:
  - Four separate interrupt requests
  - 16 interrupt sources, each with a separate interrupt-pending flag and interrupt-enable bit
- Debug support: Freeze or suspend Versatile Timer Unit activity

## INTERFACES

- AMBA 2 APB host interface
  - 16-bit read/write data buses
  - 10-bit address bus
- TIOx pins through chip I/O pads (optionally through a General Purpose I/O Controller)
- Clock interface – APB clock for registers, interrupt functions, and timer clock source
- Interrupt interface (one interrupt signal for each timer subsystem, plus combined interrupt)
- One asynchronous reset input
- Freeze/suspend interface
- DFT signals

## HARDWARE CONFIGURATION OPTIONS

| OPTION | RANGE | DEFAULT |
|---|---|---|
| Local clock gating for low-power operation | On of Off | Off |

## DELIVERABLES

- Synthesizable Verilog source code
- Integration testbench and tests
- Documentation
- Scripts for simulation and synthesis with support for common EDA tools

For more information, please contact us at ip@silvaco.com.

SILVACO
HEADQUARTERS
2811 Mission College Boulevard, 6th Floor
Santa Clara, CA 95054
Phone: 408-567-1000
Fax: 408-496-6080

CALIFORNIA sales@silvaco.com 408-567-1000
MASSACHUSETTS masales@silvaco.com 978-323-7901
TEXAS txsales@silvaco.com 512-418-2929

JAPAN jpsales@silvaco.com
EUROPE eusales@silvaco.com
FRANCE eusales@silvaco.com
KOREA krsales@silvaco.com
TAIWAN twsales@silvaco.com
SINGAPORE sgsales@silvaco.com
CHINA cnsales@silvaco.com

WWW.SILVACO.COM

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