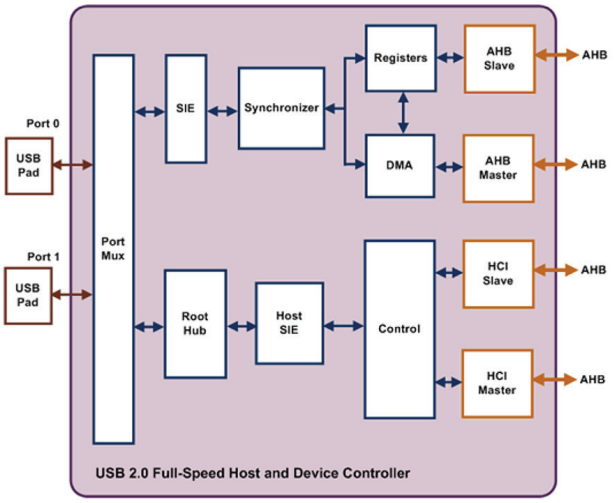
USB 2.0 Full Speed Device+Host Controller

DESCRIPTION

The USB 2.0 Full-Speed Host and Device Controller is a highly configurable, synthesizable USB core built from silicon-proven technology from NXP Semiconductors.

The core is an extremely low gate count design that provides an efficient USB implementation in cost-sensitive applications.

It integrates with standard USB transceivers on USB side and AMBA AHB interfaces on the system side, supporting all major embedded microprocessor cores.



FEATURES

- Compliant to the USB 2.0 specification
- Supports Full-Speed (12 Mbps) operation
- Host and Device functions can switch under software control
- Host is OCHI-compliant
- Two ports available as Host
- DMA engine with connection to AHB interface
- Low gate count (36K gates)
- Various low power features including LPM support
- Up to 14 non-control logical endpoints
- Bulk, Interrupt, or Isochronous endpoint types
- Maximum packet size 0-1023
- Software-controlled interrupt structure
- Supports single-port RAM for endpoint buffers
- USB buffers can be programmed at the packet or transfer level
- Supported by 3rd-party software (drivers, and so on)
- AMBA AHB-compliant system interfaces

HARDWARE CONFIGURATION PARAMETERS

OPTION	RANGE
NUM_ENDPOINTS	0-14
SINGLE_BUFF	Yes or No
DOUBLE_BUFF	Yes or No

DELIVERABLES

- VHDL RTL source code (Verilog on request)
- Test bench with test suites
- Documentation including User's Guide and Integration Guide
- Technology-independent synthesis constraints

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