I3C Dual-Role Master

SILVACO

I3C is a new a standard from the MIPI Alliance that unifies and extends the legacy interfaces of I2C and SPI and adds new powerful features to support modern mobile, automotive, and IOT applications. I3C products from Silvaco provides customers with a range of products that allow customers to take advantage of the higher performance and lower power features that come with I3C.

The I3C Dual-Role Master controller is a highly configurable I3C master that can be used in microcontroller based environments to provide I3C connectivity to any device. It contains master capabilities as well as the same features as the I3C Advanced Slave. It can be configured in a number of different ways to allow the core to use the minimum amount of logic to reduce both area (cost) and power.

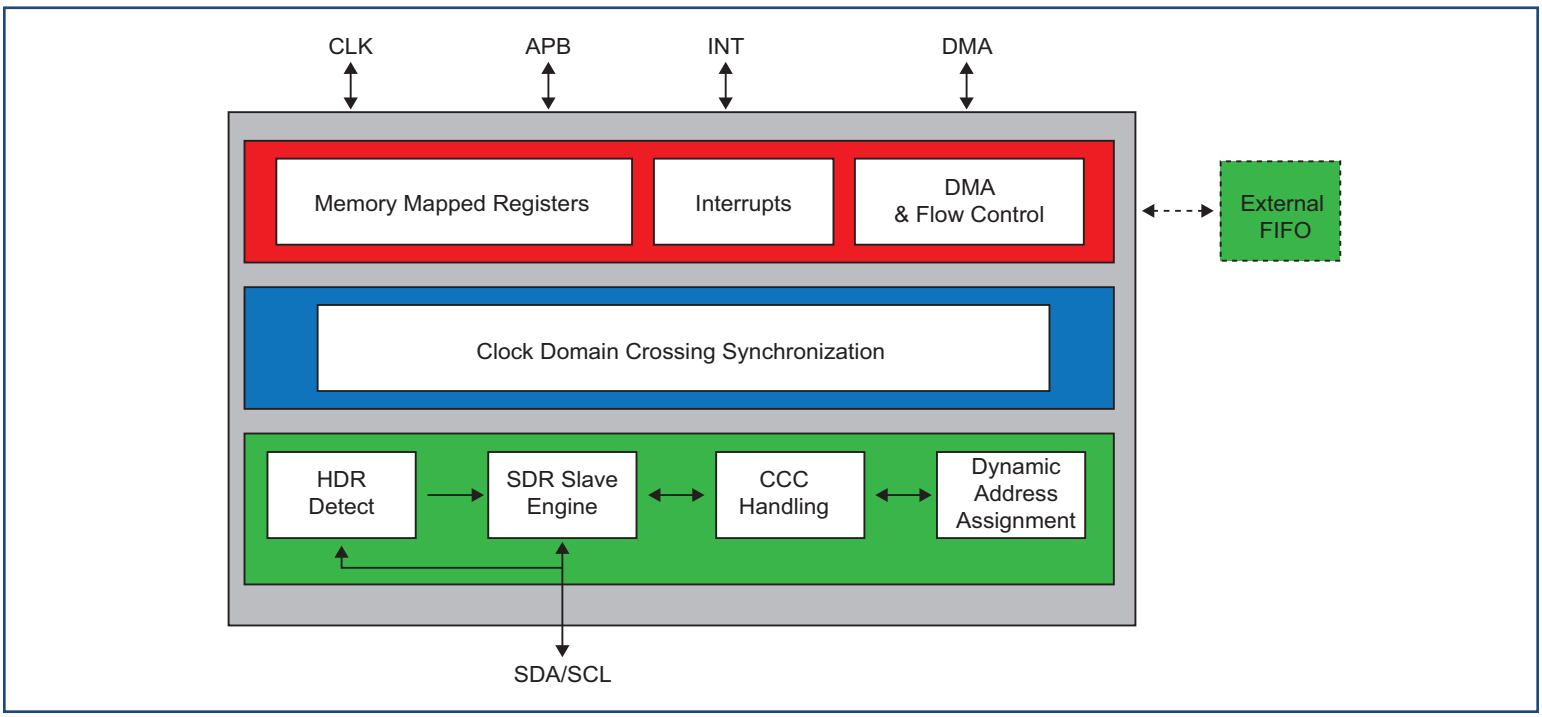
APPLICATIONS

- Mechanical sensing (Gyroscopes, MEMS, etc.)
- Environmental sensing (Light, pressure, temperature, humidity, etc.)
- Biometrics (Fingerprinting, glucose, heart rate, breathalyzer, etc.)
- Communication (Near-field sensors, infrared remotes, etc.)

FEATURES

- Highly configurable core that allows customer to minimize unneeded logic
- Compliant with the latest version of the MIPI I3C specification
  - Legacy I2C coexistence, including I2C messaging
  - Dynamic addressing
  - Multi-drop capability
  - Multi-master capability
  - Standard data rate (SDR)
  - Error detection types (S0-S6, M0-M2)
- Advanced I3C features
  - Hot join
  - Hot-join Dynamic Address Assignment
    - Secondary Master
    - SDR-only Secondary Master
  - Status I2C address support (Slave and SDR only Slave)
  - Support for I2C pads with 50ns glitch detector
  - In-band interrupts
  - Asynchronous time stamping (Mode 0)
  - High speed mode (HDR-DDR)
  - Additional CCC's (ENTAS1-2, ENEC/DISEC, SET/GET Max, GETMXDS)

BLOCK DIAGRAM



FEATURES (CONTINUED)

- AMBA APB (v3) application interface
  - Memory mapped registers
  - DMA, flow control features
  - FIFO options
    - Internal 2-byte ping-pong buffer
    - Internal FIFO (up to 32 bytes)
    - External FIFO interface
  - Slow clock option for ultra-low power operation
- Low gate count (2-5K gates, depending on configuration)

DELIVERABLES

- Verilog RTL source code
- System Verilog test bench with test suites
- System Verilog I3C Master bus functional model
- System Verilog I3C Slave bus functional model
- System Verilog I3C Bus Monitor
- Provided as source code, no additional licenses required
- Master controller (binary) for developing/testing FPGA prototypes
- Documentation including User's Guide and Integration Guide
- Technology-independent synthesis constraints

For more product information, please contact ip@silvaco.com

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