PDK-Based Analog/Mixed-Signal/RF Design Flow

August 2006

Introduction

This document describes an integrated design flow and methodology to design analog, mixed-signal, and RF (AMS/RF) ICs that achieve their performance, yield, and time-to-market goals using process design kits (PDKs). This same flow can also be used to build digital blocks such as standard cells, I/O pads and custom circuits to be used in Systems On Chips (SOCs) with millions of transistors.

The critical link between the design tool set and the target foundry process is an accurate process design kit (PDK). A PDK contains a validated set of schematic symbols, netlisting equations, SPICE models, layout technology files, parameterized cells (Pcells), DRC/LPE/LVS rule files, and parasitic extraction decks. An integrated toolset and validated PDK eliminate many of the inaccuracies and obstacles typically found in AMS/RF IC design. The development process becomes predictable from initial design decisions to final verification for tapeout.

Simucad has its roots in physics-based TCAD tools and services to foundries and integrated devices manufactures (IDMs) for process and device simulation as a part of Silvaco International. Simucad has been a pioneer in SPICE model extraction since 1984. Foundries and IDMs use Simucad's 3D physics-based inductor, bit cell, and interconnect characterization tools to generate models for their design customers. We understand the importance of accuracy. We work closely with our foundry partners to improve their processes and devices. We also work closely with our foundry partners in providing accurate, timely, validated PDKs for our mutual customers.

A complete AMS/RF design flow includes a front-end flow that enables circuit designers to easily enter circuit schematics for a bottom-up approach and HDL code for a top-down approach. Using either approach the design can be simulated at the analog, mixed-signal, RF, or full-chip level. A complete AMS/RF design flow includes a back-end flow that enables layout designers to rapidly construct, place, and verify layout that is DRC and LVS correct. The design loop is not closed until RC parasitics are extracted and included in the final

simulations at both the block and full chip levels. The Simucad AMS/RF design flow meets these requirements.

Front-end Circuit Design Flow

The bottom-up approach for the Front-End Circuit Design Flow uses a schematic editor to create device level schematics with transistors, capacitors, resistors, inductors, varactors, and other components. The schematic editor provides the ability annotate the devices with parameters such as length and width and generate netlists for circuit simulators and LVS verification tools. It manages design hierarchy. The schematic editor provides the ability to control the simulation process with SPICE corner models, circuit stimulus and setting up the required sweeps and analyses that are required to validate the circuit. The waveform viewer enables designers to view and annotate plots in both the time and frequency domains. Capabilities such as interactive DC bias back-annotation from simulator to schematic and a waveform calculator enable circuit designers to quickly analyze their designs for accuracy, performance and yield.

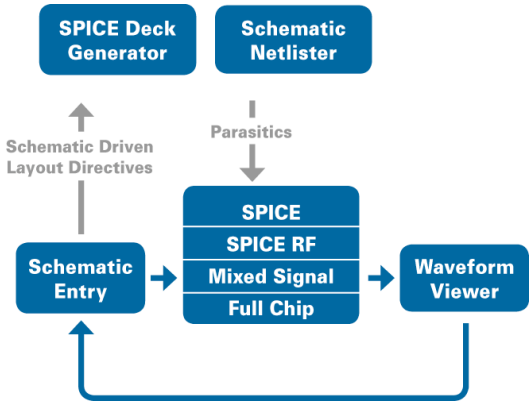


Fig 1. Front-end Flow

RF Harmonic Balance-based simulation provides a complete set of steady-state large-signal analyses and measurements to design GHz range RF ICs driven with multi-tone sources in the frequency domain. It accurately and efficiently simulates harmonic distortion, intermodulation products, gains, noise, oscillator phase noise in non-linear circuits using SPICE netlists. Shooting method-based simulation is an iterative procedure layered on top of transient analysis that is design to solve boundary-value problems. A complete RF circuit analysis requires that both the harmonic balance and the shooting method be used. It is critical that the same SPICE model interpretation, schematic netlist and DC operating solution be applied to both methods for accuracy and consistency.

The front-end flow must also manage multi-user projects with shared work-spaces for libraries of cells and symbols used by the design team.

The top-down approach uses a text editor to create behavioral models that can be simulated directly or can be synthesized down to the gate level and verified with by a Mixed-Signal simulator and a high-level language test bench. Interactive debugging of HDL design and stimulus code is critical for rapid turnaround of mixed-signal designs.

Back-end Layout Design Flow

A complete AMS/RF design flow includes a back-end flow that enables layout designers to rapidly construct, place, and verify layout that is DRC and LVS correct.

Layout designers require a fast, easy-to-use, high capacity layout editor that also has the power of scripted parameterized cells (Pcells). Pcells provide DRC correct layout for each device instantiated in the schematic. They also generate a correct LVS netlist for layout material that does not appear in the schematic such as resistor straps and guard-rings.

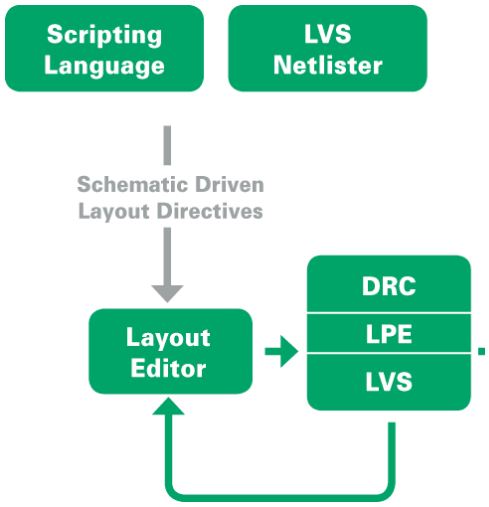


Fig 2. Back-end Flow

The critical iteration loop in the back-end layout flow is between block layout and design rule checking (DRC) and layout vs. schematic (LVS). Layout designers usually work one block at a time—placing it in a library after it is DRC and LVS correct. This workflow is tightly integrated to rapidly import, inspect, correct, and verify layout errors. The flow must also be integrated with industry standard third party sign-off DRC/LVS tool that a foundry may require.

Layout Parameter Extraction (LPE) is a critical step the LVS flow of analog and RF circuits. The extractor must be able to recognize complex devices—high voltage design uses LDMOS, lateral PNP, and circular transistors. RF design uses varactor arrays, multi-fingered transistors, and spiral inductors.

A productive LVS tools requires the ability to correlate schematics, schematic netlists, layout, and extracted netlists in a tightly integrated interactive environment. The tedious work of finding shorts and opens is automated.

Process, Device, Block Level, and Full Chip Parasitic Flows

Inaccurate calculation of parasitic capacitance and resistance often kills AMS/RF IC designs. And there is always a tradeoff between accuracy and runtime with all parasitic extraction algorithms.

Foundries use a variety of 3D physics based parasitic extraction tools for memory bit cell characterization (analyzing process tradeoffs), inductor characterization (for L and Q optimization), cell parasitics of a limited number of transitors, and interconnect characterization to build extractor rule files for full-chip extractors. In many cases, full-chip capacitance extraction is sufficient to accurately analysis the parasitic effects on a circuit. Sometimes resistance is also required. It depends on the circuit, the design, and the process.

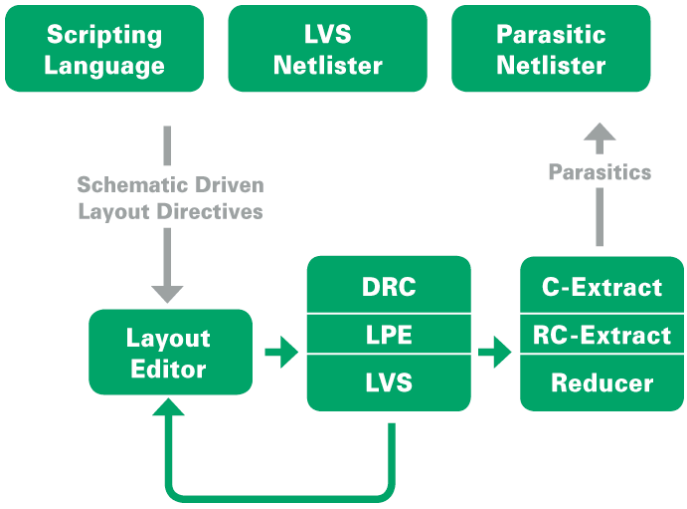


Fig. 4 Parasistic Flow

When resistance is a factor, a reduction algorithm is usually required to reduce millions of R's and C's into equivalent Pi networks, T networks or transmission lines.

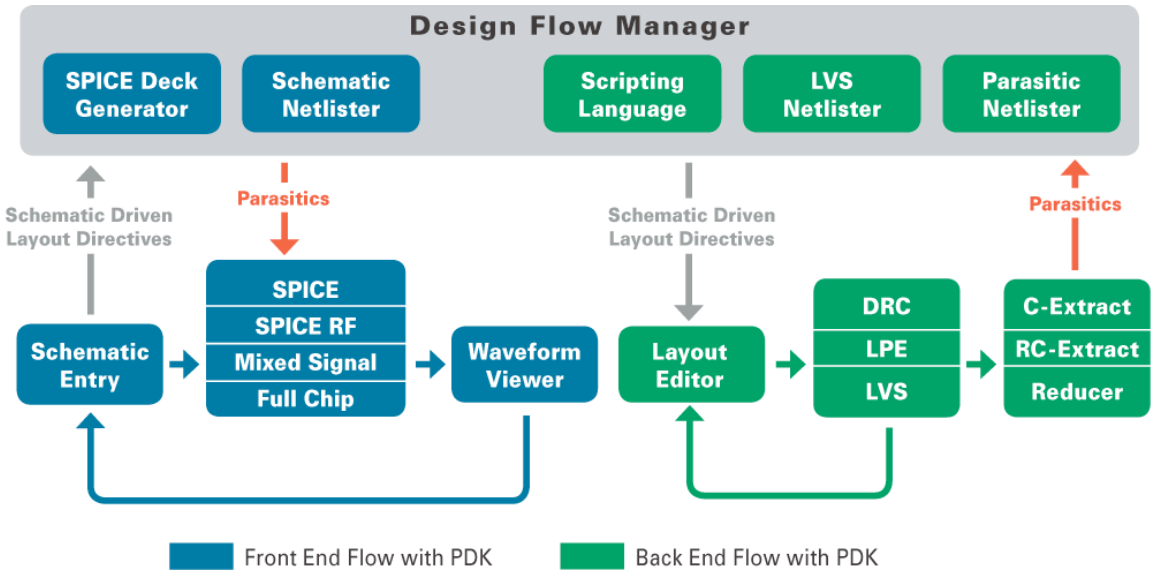
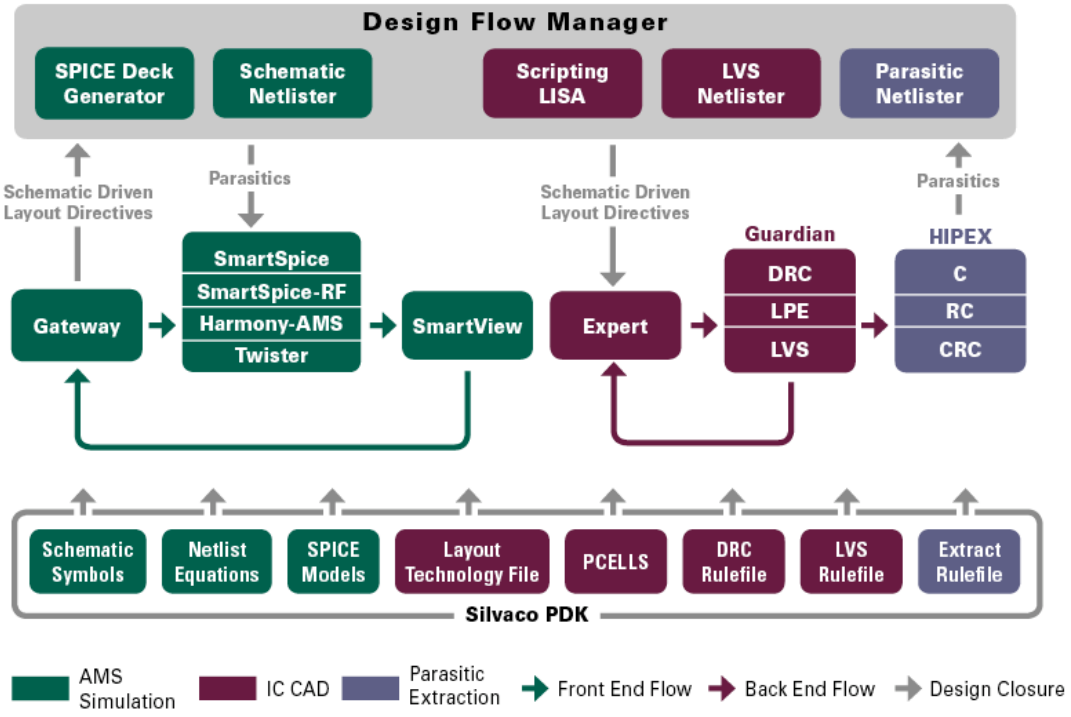


Fig. 5. Parasitic Loop

Process Design Kit (PDK) Components

A PDK provides the integration and consistency to create a predictable and stable design flow out of a set of EDA tools for a specific semiconductor process. It must also be flexible enough to accommodate process revisions and derivatives. A PDK contains a validated set of schematic symbols, netlist equations, SPICE models, layout technology files, parameterized cells (Pcells), DRC/LPE/LVS rule files, and parasitic extraction decks.

A PDK jump-starts a design team with an instantly productive environment and ensures manufacturing success with pre-configured schematic symbols, integrated SPICE models and validated technology files. A PDK reduces costly rework cycles caused by assumptions and design data mismatch. It tightly links EDA tools, IC designers and foundry support for fast time-to-market.



Simucad and its foundry partners develop and validate PDKs for download from the foundry website or the Simucad secure website. They maintain PDKs over process changes and extend them to accommodate process derivates. Because of the architecture of the Simucad AMS/RF tool set, Simucad PDKs are significantly easier to develop and maintain than technology files from other legacy design software.

Simucad can support PDKs for CMOS, Bipolar, BiCMOS, LDMOS, BCD, SOI, SiGe, GaAs, TFT, CCD and other processes.

Foundry Partners

Simucad has a partnership program with leading AMS/RF foundries to provide and support PDKs for mutual customers.

These foundries supply Simucad with the current design data to develop PDKs and work with us to validate the PDK integrity of the tapeout flow.

Foundry-Specific PDKs Available - NDA Required

AMI	C5 (0.6u CMOS 40V)
	2T100 (0.7u CMOS, 40V)
ASI	AS180FF (0.18u SOI)
Jazz	SBC18HX (0.18u SiGe RF)
	BCD (0.5u BCD 40V)
	BP30 (1.25u Bipolar)
STARC	(90nm CMOS)
Tower	TS18 (0.18u CMOS 5V)
TSMC	CM013RF(0.13u CMOS Logic, Analog, RF)
	CM018RF (0.18u CMOS Logic, Analog, RF)
UMC	RFCMOS018 (0.18u CMOS Logic, Analog, RF)
X-Fab	XC06 (0.6u CMOS 60V)
	CX06 (0.6u CMOS)
ZMD	C7B (0.6u BCD)

Reference Design PDKs Available - No NDA Required

MOSIS SCMOS Design Kit
Analog, Mixed-Signal, RF, and Logic Simucad PDKs

Tools in the PDK-based Simucad AMS/RF Flow

The design flows described in this document are based upon the following EDA software tools from Simucad. Please contact your Account Manager or see datasheets and technical papers at www.Simucad.com.

Gateway Schematic Editor is the front-end of the Analog/Mixed Signal/RF IC Design Platform. It is tightly integrated with Simucad's circuit simulation, digital simulation, layout, DRC, ERC, LVS, and parasitic extraction tools. Advanced hierarchical editing features are available on Unix, Linux, and Windows.

SmartSpice Analog Circuit Simulator delivers the highest performance and accuracy required to design complex analog circuits, analyze critical nets, characterize cell libraries, and verify analog mixed-signal designs. SmartSpice is compatible with popular analog design flows and foundry-supplied device models.

SmartSpice-RF Harmonic Balance Based Simulator provides a complete set of steady-state large-signal analyses and measurements to design GHz range RF ICs driven with multi-tone sources. It accurately and efficiently simulates harmonic distortion, intermodulation products, gains, noise, oscillator's phase noise in non-linear circuits using SPICE netlists

Harmony Analog/Mixed-Signal Simulator combines accuracy, performance and capacity with the flexibility of simulating circuitry expressed in Verilog, SPICE, Verilog-A and Verilog-AMS. Harmony single-kernel analog/mixed-signal simulator dynamically links in the capabilities of the SmartSpice Circuit Simulator and SILOS Verilog Simulator at run time.

Expert Layout Editor enables mask designers to achieve maximum density and performance in analog and digital layouts. Expert's high-productivity design environment offers fast layout viewing, full editing features, large capacity, and powerful scripting for automation with parameterized cells (Pcells).

Guardian DRC/LVS/LPE Physical Verification products provide interactive and batch mode verification of analog, digital, and mixed signal IC designs. Seamlessly integrated with Simucad schematic capture and layout editor, these tools efficiently perform design rule checks (DRC), layout vs. schematic (LVS) comparisons, and layout parameter extractions (LPE).

HIPEX Full-Chip Parasitic Extraction products perform 3D-accurate and 2D-fast extraction of parasitic capacitors and resistors from hierarchical layouts into hierarchical transistor-level netlists using nanometer process technology. They are tightly integrated with the Expert Layout Editor for the complete design flow of DRC/LVS/LPE and RC parasitic extraction on one platform.

Importing Legacy Data from other EDA Flows

Many people use legacy designs as a starting point when designing new circuits and chips. Simucad makes it easy to migrate legacy designs to the Simucad AMS/RF Design flow using industry standard design data formats whenever possible. We also deliver proven data translators to convert third party EDA vendor data to formats understood by Simucad Tools.

Data Format of Design Tool	Simucad Compatibility
Schematics	EDIF 2 0 0 Import into Gateway
Layout Editor Tech Files	Expert reads Virtuoso™ files
Layout Data	Expert reads/writes GDSII
DRC/LVS Decks	Guardian translates Calibre™ and Diva/Dracula/Assura™
SPICE models	SmartSpice reads HSPICE™
SPICE netlists, commands	SmartSpice reads HSPICE™

Simucad Services Available

Simucad offers engineering services to help customers become instantly productive using our EDA software tools.

SPICE Model Extraction Services provide accurate, high quality SPICE models for analog, digital, mixed-mode and RF applications supporting all commercially available SPICE models. Extraction of DC, AC (s-parameters), Capacitance, Temperature, and Noise SPICE parameters from either packaged parts or wafers is acceptable. Temperature ranges from -55°C to + 150°C with worst case and corner model generation. Fast turnaround is available.

PDK Development Services jump-start analog and mixed-signal design teams and the CAD teams who support them with all of the foundry-specific models, symbols, rule decks and parameterized cells (P-cells) required for rapid, sustainable success using the complete Simucad AMS/RF IC design toolset.

IC CAD Services jump-start analog and mixed-signal design teams with CAD flow integration, conversions of rule files/runsets, and full-chip verification using the Simucad custom IC design toolset. This service provides a painless transition from legacy EDA and design data to an integrated Simucad tool flow.

Parasitic Extraction Services provide solutions for customers who have occasional cell level passive element and parasitic modeling requirements or have a need for integrated IC CAD/extraction solutions. All extractions are physics-based—not rule based, so novel structures can be analyzed accurately for all coupling effects.