Utmost IV SPICE Optimization Module

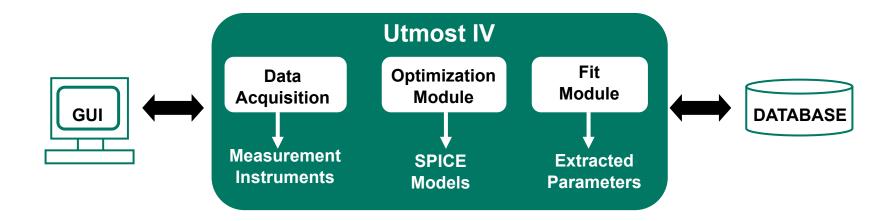


SILVACO

Utmost IV Architecture



 Utmost IV is a 'database' based product unlike Utmost III and competitors which are file based





Optimization Module Overview

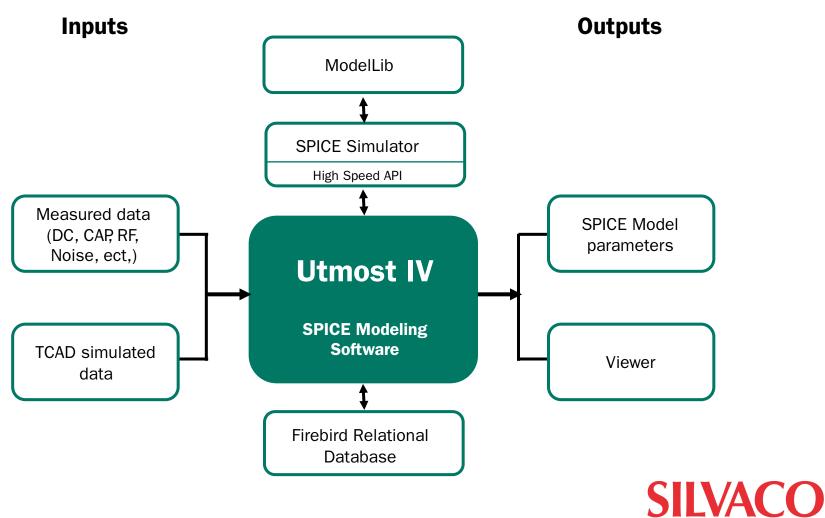


- Unlimited Multi-target Optimization
- Full Macro-model Support
- Family of Advanced Optimizers
- High-speed SmartSpice Interface
- Technology Independent
- Flexible Data Format
- Underlying 64-bit Relational Database



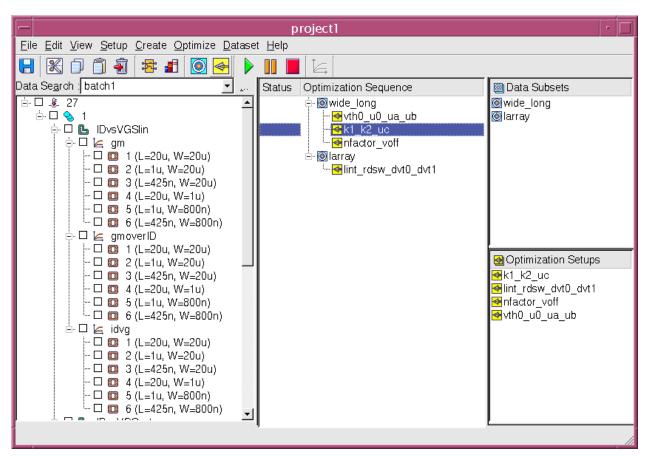
Utmost IV Optimization Module Architecture





Utmost IV is Project Organized



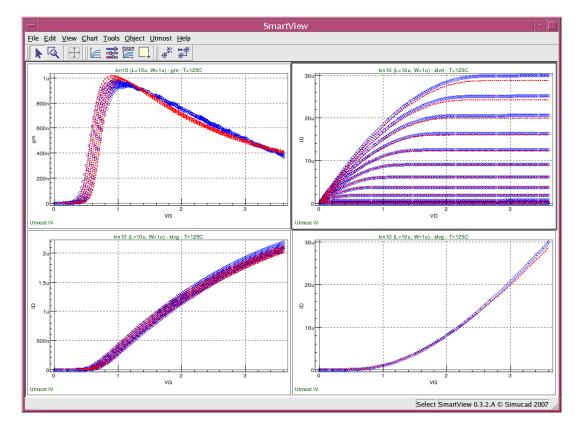




Multi-Target Optimization



 Any combination of data can be used as the target for an optimization

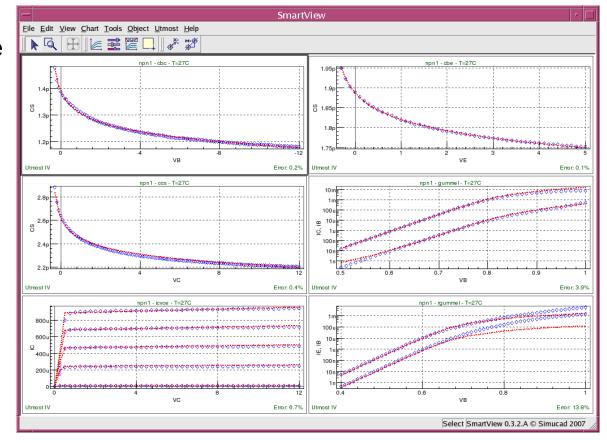




Multi-Target Optimization 2



 Multiple temperatures, mix dc and ac, multiple batch or wafers





Family of Advanced Optimization Algorithms

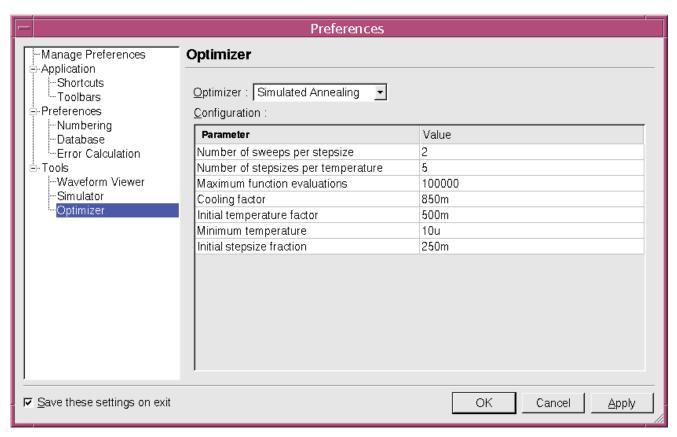


- Local (traditional) optimizers are fast, but need good starting point
 - Levenberg Marquartz
 - Hooke-Jeeves
- Global (next generation) optimizers run more iterations, but require less conditioning
 - Genetic Algorithm
 - Simulated Annealing
 - Parallel Tempering
 - Differential Evolution



Easy to Select and Configure Optimizer



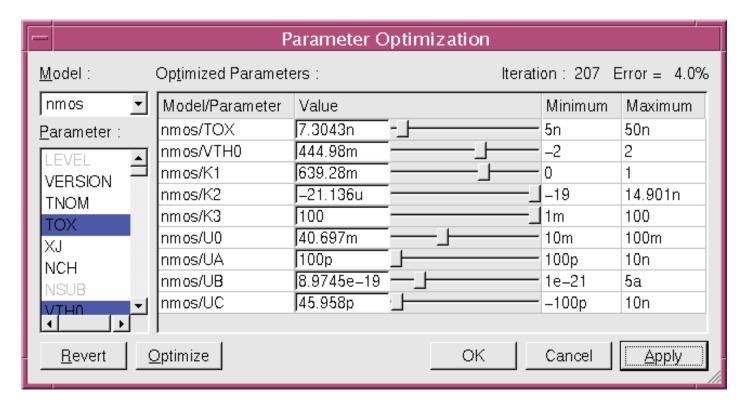




Rubberband Optimization



No limit to number of parameters

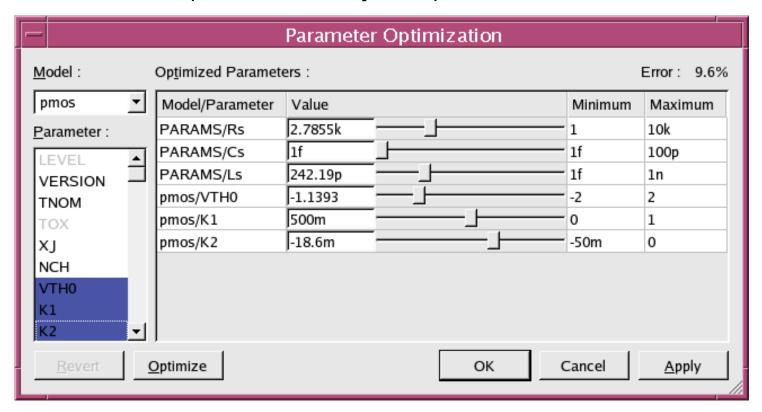




Rubberband Optimization 2



Parameters for multiple models may be optimized at the same time





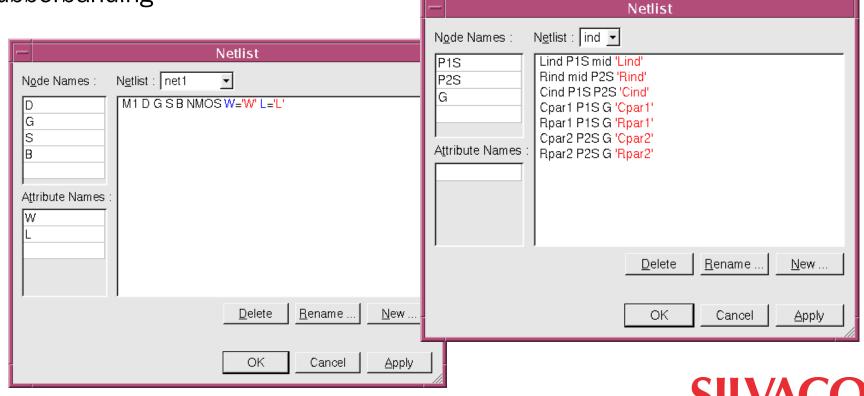
Macro-Model Optimization



Netlist of any complexity can be defined for macro-model

All macro-model parameters available for simultaneous optimization and

rubberbanding



High Speed SmartSpice Interface



- Simulation is provided using the full power and flexibility of SmartSpice
- Very fast simulation times provided by high speed API interface
 - 80 dc simulations per second on AMD Athlon64 X2 4800
- No significant loss in speed when using macro-model instead of compact model
- Optimization time for typical LDMOS macro-model
 - Utmost III approx. 1.5 2.0 hours
 - Utmost IV approx. 2-3 minutes



ModelLib Saves the Day



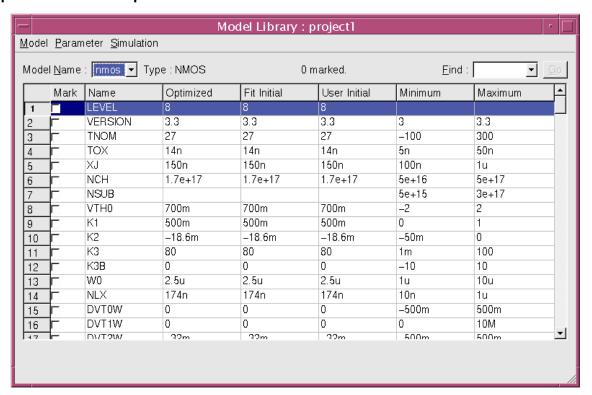
- Utmost IV no longer contains the models
- Model information provided by ModelLib in SmartSpice
- No difference between SPICE simulator and model extractor is possible
- Any new SPICE models in SmartSpice are also instantly available to Utmost IV
- Web-based and web-delivered model updates



Store all your Models in the Model Library



- No limit to number or type of models
- Versatile import and export

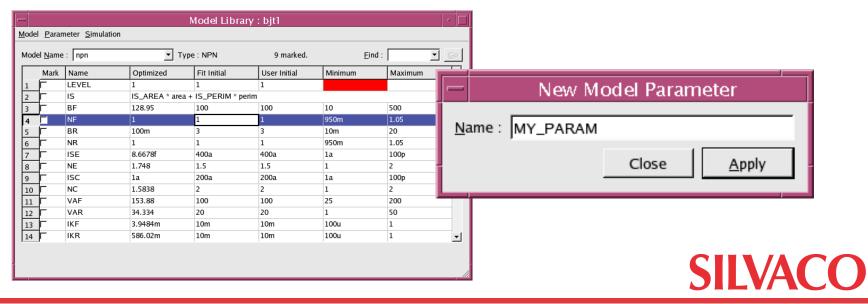




Model Customization and Development Environment



- Use equations to specify model parameters
- Develop scalable custom macro models
- Using SmartSpice model development environment your own SPICE models
- Instantly add new model, new parameters, verify in Utmost IV and develop model extraction sequence in parallel



Technology Independent



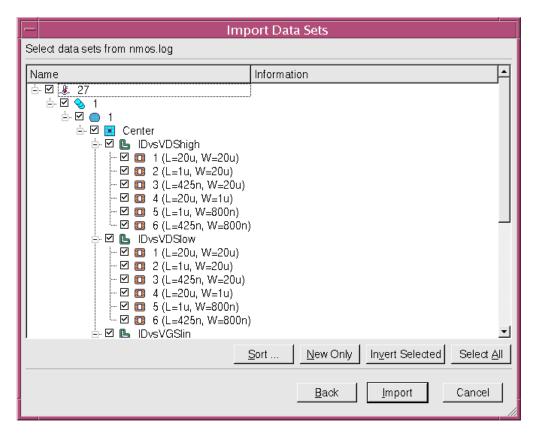
- No more BIP, MOS, SOI, SPICE model modules to buy like in Utmost III and competitors' software
- No limit to number of name of device nodes
- Supports all types of semiconductor devices
- All spice model types available through SmartSpice



Flexible Data Format



- Dataset import for legacy Utmost III logfiles
- Flexible dataset import using Utmost IV datafiles
- No longer any requirement for data to have equally spaced points
- Sweeps can be linear or logarithmic, or simply a list of values

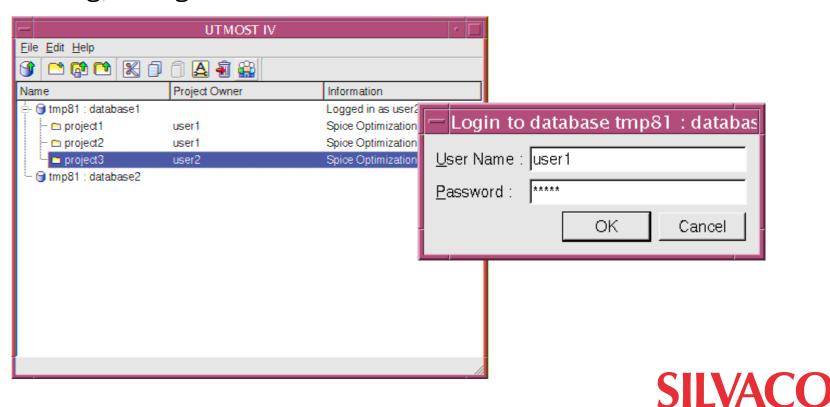




64-bit Relational Database



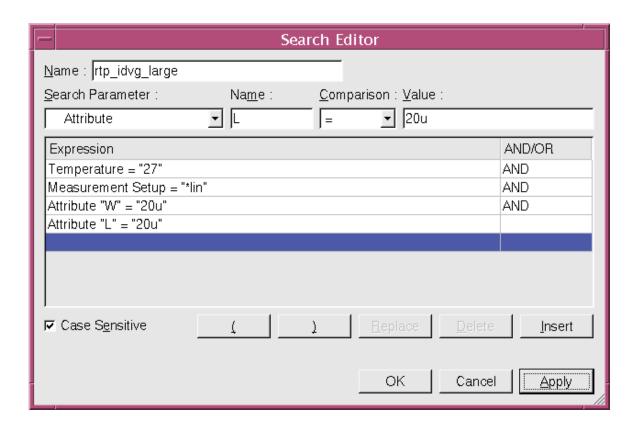
- Multi-user, multi-access Firebird 64bit relational database organises your work
- Data sharing, storage and retrieval



Search Editor



Database search allows you to retrieve and share information

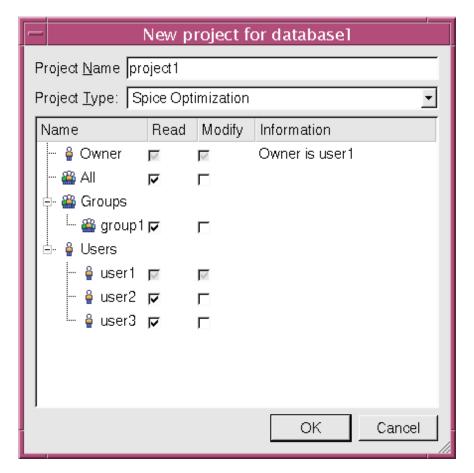




Database Permissions



 Full access control for data security





Conclusion



- Utmost IV Optimization Module provides an easy to use, database-driven environment for the generation of accurate, high quality SPICE models and macro-models for analog, mixed-signal and RF applications
- Utmost IV provides model extraction solution for problems that were not possible to solve with Utmost III and competitors' software
 - Deep sub-micron CMOS with the new generation of SPICE models (HiSIM, PSP, Dual Gate, BSIM, etc.)
 - Complex power MOS/Bipolar macro-models
 - Passive and active RF macro-model (varactor, inductor, etc.) s-parameter optimization
- Utmost IV allows parallel development of device models for SPICE applications and model extraction strategies

