TFT 2D/3D Simulation

Amorphous and Polycrystalline Device Simulation
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• TFT 2D/3D is an advanced device technology simulator equipped with physical models and specialized numerical techniques required to simulate amorphous or polysilicon devices
• Planar and non-planar device modeling is possible implementing advanced TFT 2D/3D models focusing on defects and defect states
• TFT 2D/3D can be coupled with the Athena process simulator for realistic device properties
• The accurate modeling of these defects and the density of defect states is critical for accurate predictive software
The TFT 2D/3D module models the electrical effects of these properties through accurate mathematical and experimentally proven default equations.

The properties of the defect states in the material’s band gap can be easily adjusted by specifying activation energy, capture cross-sections or lifetimes for electrons and holes.

General expressions for defect and density of states can however prove inadequate as the knowledge of defects and their distributive properties improves.
• The TFT 2D/3D overcomes this problem by providing an ANSI C compatible C-Interpreter and debugging environment.
• This permits implementation of in-house expressions to account for these effects.
• Mobility, impact ionization, band-to-band tunneling, trap-assisted tunneling and trap assisted tunneling with Coulombic wells (Poole-Frenkel effect).
• These factors can be easily modified by the user to accurately predict device performance.
Applications

- Active matrix liquid crystal display (AMLCD) used in large area flat-panel displays
- Electrical characterization of non-planar or multi-gate TFT structures
- Static random access memory (SRAM) cells
- Polysilicon single grain channel TFT
- Investigating multi grain boundary effects
- Investigating influential parameters effecting mobility
• This illustrates a non-planar TFT created in Athena
• This type of device is used for driving an active matrix display element
• Contours of the electric field are displayed
• The distribution of defects is specified by the user as a function of energy.
• This plot illustrates the different donor and acceptor trap density levels.
• Users can easily modify these trap definitions to specify material characterizations.
• Atlas models the reverse leakage at negative gate biases resulting from band-to-band tunneling
• Shown is a plot of the high reverse leakage for two different drain biases
• This Illustrates TFT structure creation using the layout/ process simulation interface

TFT layout definition.

Cross-section definition.
• Athena uses the layout and cross-section definitions to create the TFT structure
• The width and length can be modified easily by changing the layout and cross-section definitions
These curves show the $I_D/V_D$ curves for a 200µm width 150µm length TFT.

These curves show the $I_D/V_D$ curves for a 10µm width/10µm length TFT.
• Non-isothermal behavior can also be simulated
• Non-planar buried gate advanced 4µm channel polysilicon TFT used in AMLCD circuits
• Extended LDD regions improve electrical performance
• Ion implantation and diffusion modeled within Athena
• Density of states within bandgap implemented using C-interpreter
• Input deck written using DeckBuild
• go atlas invokes Atlas to perform electrical characterization
• Density of states are specified using defect statement and defect1.c file
• Interface charge and mobility models can also be specified
• Numerical models include band to band tunneling and Poole-Frenkel effect
• Typical in-house density of states expressions for the acceptor and donor like defect states within material bandgap

• Double exponential expresses both shallow and deep level traps

\[
D(E) = N_{\text{tail, DON}} \exp \left[-\frac{\text{energy}}{E_{\text{tail, DON}}} \right] + N_{\text{deep, DON}} \exp \left[-\frac{\text{energy}}{E_{\text{deep, DON}}} \right].
\]

\[
D(E) = N_{\text{tail, ACC}} \exp \left[-\frac{\text{energy}}{E_{\text{tail, ACC}}} \right] + N_{\text{deep, ACC}} \exp \left[-\frac{\text{energy}}{E_{\text{deep, ACC}}} \right].
\]
• Density of states for 4μm gate polysilicon TFT device for AMLCD technology
• Shallow and deep level traps are shown
• Parameters easily altered by changing C function file
As deposited film grows and coalesce into grains several factors in addition to grain boundaries can affect electron and hole mobility. In particular, surface roughness can significantly impede the electron and hole mobility through the channel especially at high electric fields. TFT 2D/3D together with Atlas helps to model this effect accurately through several mobility models. Of particular interest here is the Lombardi CVT model invoked using the keyword cvt on the models statement line. Using this model allows good agreement between experimental results and those predicted by the simulation.
• The Lombardi CVT model is based on the surface roughness $\mu_{sr}$
• The surface roughness $\mu_{sr}$ has proportional constants which are the surface roughness for electrons $\mu_{sr,n}$ and holes $\mu_{sr,p}$
• The electron and hole surface roughness components are expressed as

$$
\mu_{sr,n} = \frac{\text{deln.cvt}}{E_\perp^2} \quad \text{and} \quad \mu_{sr,p} = \frac{\text{delp.cvt}}{E_\perp^2}
$$

• Here $E$ is the perpendicular electric field to the channel
• deln.cvt and delp.cvt can be user defined away from default values specified on the models statement line
• Simulation of 4µm gate polysilicon TFT device for AMLCD technology
• Experimental raw data is shown in red
• Simulation data is shown in green
• Excellent agreement is clearly seen
Simulation of 4μm gate polysilicon TFT device for AMLCD technology reverse and forward bias

Experimental raw data is shown in red

Simulation data is shown in green

Reverse leakage current is insufficient for small negative voltages which can be increased using the Poole-Frenkel effect
• The Poole-Frenkel effect enhances the emission rate for trap-to-band phonon assisted tunneling and pure thermal emissions at low electric fields

• The Poole-Frenkel effect occurs when the Coulombic potential barrier is lowered sufficiently due to the applied electric field

• The Poole-Frenkel effect is modeled by including field effect enhancement terms for Coulombic wells and thermal emissions in the capture cross sections

• This model also includes the trap assisted tunneling effects in the Dirac well

• The model is invoked by specifying the commands trap.tunnel and trap.coulombic on the models statements
• It can be seen that by including the Poole-Frenkel effect the leakage current has been increased.
• Parameters can be furthered tailored to improve the agreement between experimental and simulated data.
• Impact ionization occurs from collisions between energetic free carriers and atomic lattice generating more free carries.
• This is specified using the keyword `selb` on the impact statement line which uses Selberherr’s impact ionization model.
• Impact ionization is seen to increase as the drain bias increases.
• Grain boundaries severely affect the mobility in thin film transistors
• Grain boundaries can be assigned within the channel as different regions
• These regions can then be assigned different properties away from the common properties of the grain
• The properties can be supplied from a C-interpreter file or using functions within TFT 2D/3D
• TFT can be used with MixedMode to accurately simulate a pixel of a TFT LCD panel
• MixedMode permits TCAD device modeling and SPICE modeling in unison
• As a more physically based alternative to compact TFT models, this allows designers to analyze and optimize LCD panel circuit designs and to evaluate the effects of parasitic components within each pixel
• TFT 2D/3D handles multiple pixels to allow large scale simulation of the LCD panel
• Shown at the left is an equivalent circuit of a TFT pixel
• MixedMode is used to simulate the electrical characteristics of the TFT driven pixel
• This illustrates the effect of bit line programming of a TFT pixel
• Drain voltage follows source voltage with a delay resulting from the external resistive and capacitative elements
• TFT 2D/3D can be used with Luminous to simulate thin film solar cells made from amorphous silicon
• Luminous is a optical simulator which accounts for optical generation and recombination in addition to coherence effects
• Spectral, DC and transient responses can be extracted from run time simulations
• A simple thin film amorphous Si solar cell is shown
• This device has an opaque metal contact in the center of the structure
• Photogeneration rates in the device are shown
• Terminal currents can be evaluated to determine quantum efficiency of the cell
• TFT 3D uses similar techniques as TFT 2D but with added third dimension and complexity
• Coupled with TonyPlot 3D powerful 3D imaging and analysis is possible.
• Here a simulation of an octagonal array of TFT elements using TFT 3D is shown
Silvaco’s advanced TFT 2D/3D device simulator has been discussed.
Polysilicon and amorphous silicon can be simulated by accurately expressing the density of states with bandgap.
Grain boundary and grain boundary effects can be simulated and analyzed.
C-Interpreter interface allows user-defined parameters to be specified.
TFT 2D/3D can run seamlessly with Silvaco’s other TCAD tools such as MaskViews and Athena.
Ease of use within the DeckBuild and TonyPlot environment.
TFT 2D/3D is fully compatible with other Atlas modules such as Luminous 2D/3D, MixedMode 2D/3D and Giga 2D/3D.