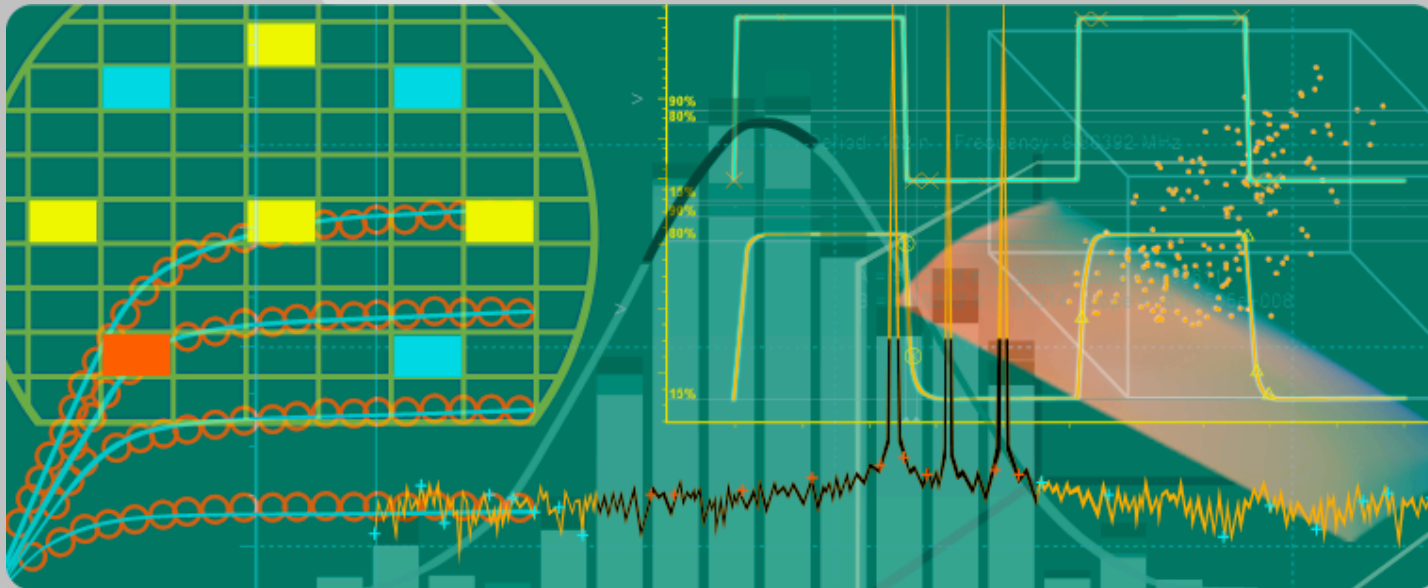
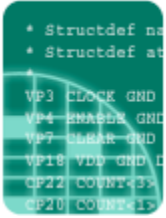


# Silvaco Level=88 Model for High Voltage Process

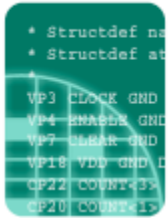


Advanced High Voltage CMOS Model



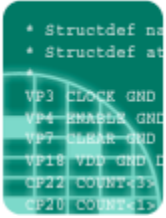
## Silvaco Advantage for High Voltage

- Silvaco is the world leader in high voltage process and device simulation (and other special processes)
  - TCAD tools simulate electrical, thermal, quantum, optical effects
- BSIM3 based Level 88 has the best high voltage model
  - UTMOST III Model Parameter Extraction Software seamlessly integrated with SmartSpice
  - Features include:
    - self-heating
    - forward and reverse mode
    - asymmetry of parasitic
    - bias dependent of the Rds
- Silvaco provides a comprehensive modeling service



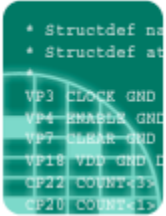
## Level=88 HV MOS Model – Overview

- Level=88 HV MOS model was developed and implemented with SmartSpice/UTMOSTIII in 1998 based on BSIM3v3 and the advanced model has been used by many companies in the world
- Core parameter set is based on a final version of BSIM3v3, namely v3.2 that ensures better continuity in the drain current equation and stable convergence property
- Additional model parameters added to the core model to express HV device-specific physical effects
- Easy parameter extractions for modeling engineers who are familiar with BSIM3v3 and also each of the HV-specific model parameters is explicitly explained in Modeling Manual by showing equations in which each parameter is used
- Extension to asymmetric source/drain device structure
  - Based on HSPICE-compatible ACM(Area Calculation Method)
  - Symmetric structure by default but different parameters for source and drain sides can also be set



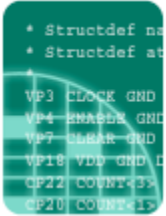
## Level=88 HVMOS Model Features

- Nine additional parameters provide the following physical effects:
  - Self-Heating
  - Asymmetry and bias ( $V_{ds}$ ) dependence of external resistance  $R_{ds}$
  - Dependence of mobility degradation on  $V_{ds}$
  - Subthreshold slope and reverse short-channel effect
  - Dependence of  $V_{sat}$  on  $V_{gs}$  and  $V_{bs}$
  - Transconductance  $G_m$  reduction in saturation at high  $V_{gs}$
  - Bias dependent saturation velocity
  - Asymmetry of all parasitics (Diodes and Resistance)
  - Forward and reverse modes of operation



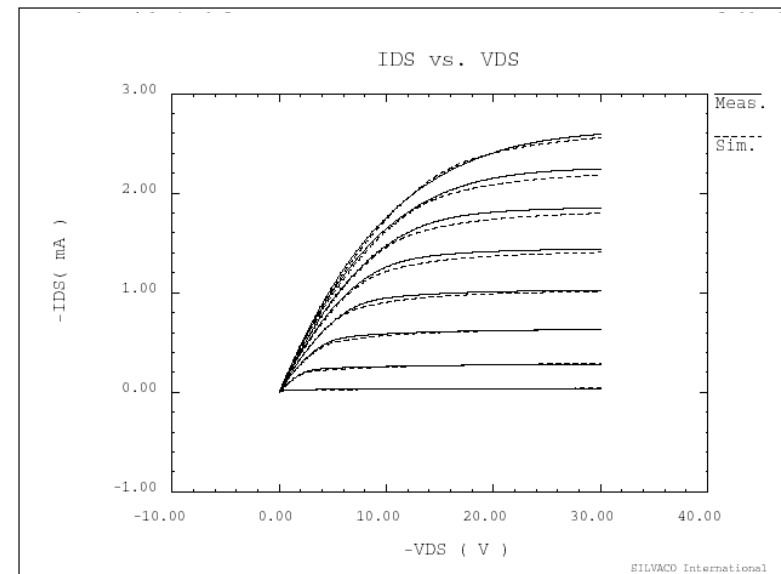
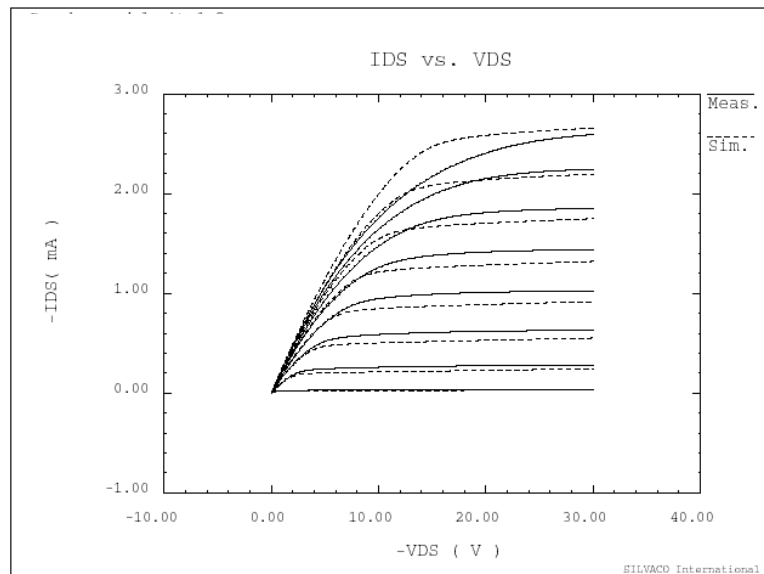
## Level=88 HVMOS Model – Additional Parameters

Parameter	Description
PRWD1	First order Vds dependence of external resistance Rds (Forward Mode)
PRWD2	Second order Vds dependence of external resistance Rds (Forward Mode)
PRWS1	First order Vds dependence of external resistance Rds (Reverse Mode)
PRWS2	Second order Vds dependence of external resistance Rds (Reverse Mode)
UD	Vds dependence of mobility degradation
PCSE	Subthreshold slope and reverse short channel effect parameter
CCSE	Subthreshold slope and reverse short channel effect parameter
VSATG	Vgs dependence of VSAT
VSATB	Vbs dependence of VSAT



# Level=88 HVMOS Model - IDS vs VDS Characteristic

P-channel, L=3.0um / W=11.0um  
VDS : 0v - 30v  
VGS : 2,4,6,8,10,12,14,16V



Measured vs simulated plots obtained with BSIM3v3(left) and Silvaco HV MOSFET(right)

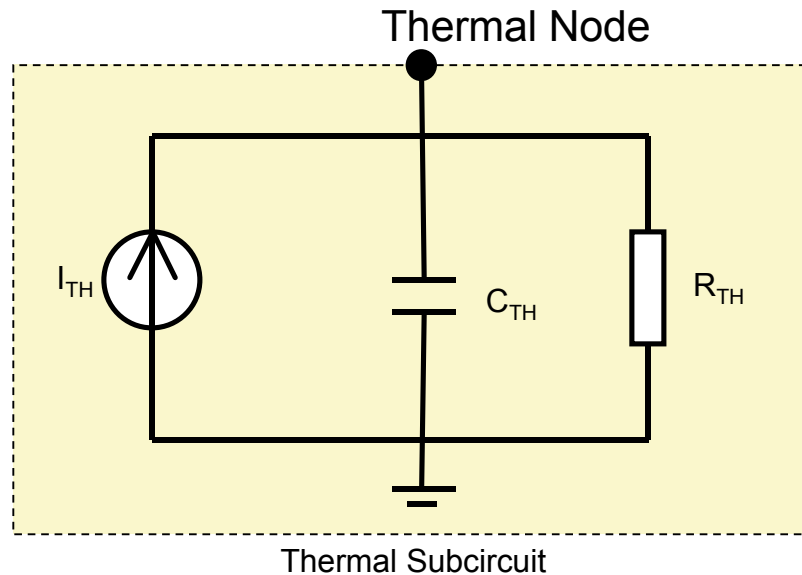
```

* Structdef na
* Structdef at
VP3 CLOCK GND
VP4 ENABLE GND
VP7 CLEAR GND
VP18 VDD GND
CP22 COUNT433
CP20 COUNT417

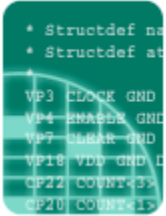
```

# Level=88 HVMOS Model – Self-Heating Effect

- Temperature rise taken into account due to self-heating effect
  - Dissipated Power :  $P_{TH}(\text{watt}) = I_{DS} V_{DS}$
  - Temperature rise :  $T_{DEV} = R_{TH} P_{TH} + T_{CIRCUIT}$
  - Affects all temperature equations in HVMOS model

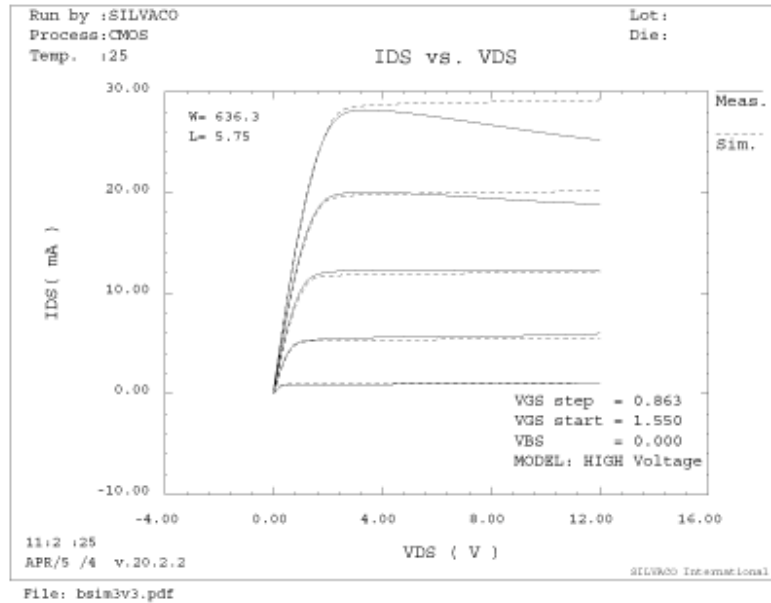


Parameter	Description
SHMOD	ON/OFF flag
RTH	Thermal Resistance [W/deg C]
CTH	Thermal Capacitance [deg C/(W_s)]

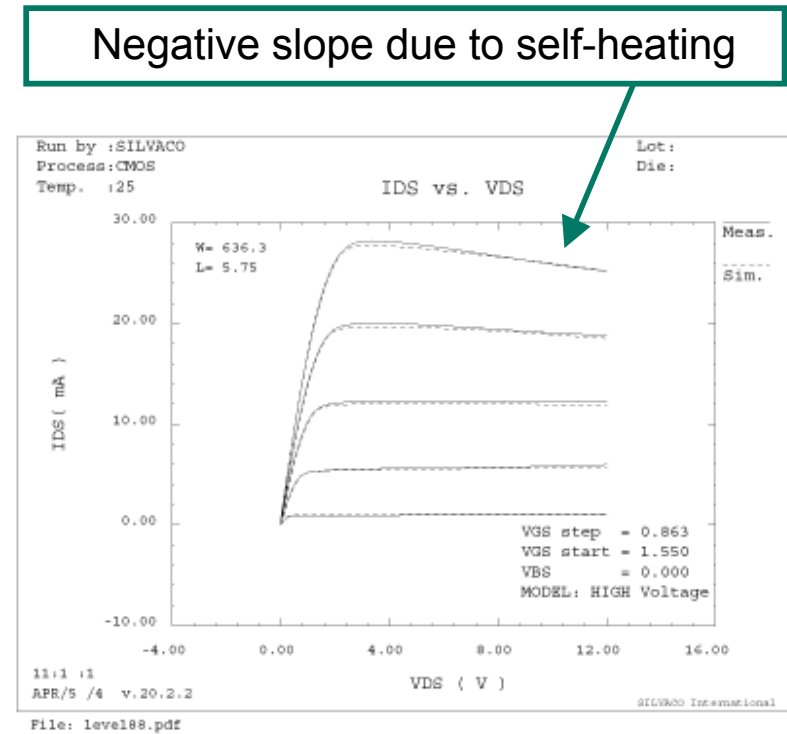


# Level=88 HVMOS Model – Self-Heating Effect

## IDS vs. VDS



Without self-heating effect  
(SHMOD=0: turned off)



Negative slope due to self-heating

With self-heating effect  
(SHMOD=1: turned on)