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What is Guardian NET?

- Performs accurate device parameter extraction from hierarchical IC designs with nanometer process technology into hierarchical transistor-level netlists
- Guardian NET is a full-chip hierarchical extractor capable of processing multimillion designs
- Tightly integrated with Guardian DRC/LVS and HIPEX parasitic extractors within Expert IC design environment
Key Features

• Exploits design hierarchy for shorter run times, more compact netlists, and less memory consumption
• Doesn’t impose any design restrictions. It can work on any shape and any angle layout. Supports designs with cell abutments, overlapping cells, and doesn’t force you to declare the cell pins or assign names to cell pins
• Design technology and style independent. Supports Dracula, Calibre, and Diva rule files
• Performs electrical rule checking (ERC) for opens, shorts, and dangles
• Efficient memory usage for handling large designs
• Tightly integrated with Expert Layout Editor to speed up the iterative process of physical verification
• Annotates layouts with nodal information enabling such advanced features as Node Probing, Node Search, and Short Locator within Expert IC design environment
Running Extraction

- Select View>Toolbars>LPE to activate LPE toolbar
- Use LPE toolbar for quick access to the extraction menu commands
- View the detailed log of the run in progress and after the extraction is complete
- Setup all the extraction options and rules within one dialog panel
- Use categorized setup pages for quick access to the options you need
- Create your own option presets using Save and Load buttons
Layout Annotation

- Highlight nets and devices by a mouse click or name search (Node Probing and Node Search)
- Maintains references to the original layout geometries
- Allows interactive navigation through net geometries
- Writes SPICE statements over device bodies
- Places all the device labels into special layer
- Fits labels automatically to device bodies or uses the specified fixed size
Guardian NET Layout Netlist Extractor

- Distinguishes between global, local, and port text by GDSII data types of containing layers
  - Global texts label nodes in the entire layout
  - Local texts label nodes in a cell
  - Port texts label ports in a cell

- Prepends instance names to local text from lower cells for distinguishing multiple copies of the same cell
Node Naming

- Define unique hierarchy level separator to avoid conflicts with your LVS program
- Specify global node names, such as power and ground
- User virtual names for unfinished nets on earlier design stages
Electric Rule Checking (ERC)

- Short or disconnect open nodes
- Output dangle nodes into a separate GDSII file
- Uses design text for ERC
- Reports local and global opens
- Reports shorts
- Report dangles

Define soft layers (typically the bulk layers) and check signal integrity on those layers.

- Report dangle nodes
- Output dangle nodes
- Netlist subcircuit dangle pips

- Rename opens
- Short open global pins (VDD, VSS, ...)

- Report BJT devices with shorted base and collector
- Report MOSFET devices with shorted source and drain

--- RULEX-E-HHOPEN: Multiple unconnected nodes with name vddq in cell TTLBF
  * RULEX-E-HLSEGMENT: Segment vddq[L] appears in cell TTLBF, LUSTEXT at [20530, 21180].
  * RULEX-E-HLSEGMENT: Segment vddq[L] appears in cell TTLBF, LUSTEXT at [19880, 92150].

--- RULEX-E-SHORT: Using in (L) at [24350, 60390], FLAT[7094070, 59290] in cell KINGSTL.

--- RULEX-E-HDANGLE: Dangling node outb appears in cell TTLBF, LUSTEXT at [36520, 37490]
Filter hcells or cells to explode using name patterns

Set a particular option for all the filtered cells

Check the layout hierarchy for violations to determine automatically which cells to explode

Explode, flatten or ignore specific cells for avoiding hierarchy violations or speeding up the extraction

Set hcells to conform with your schematic

- Fuse wiring cells automatically

- Use filter

- Show cells that match

- Hide cells that match

- The expression is well-formed

- Set all

- Checker...
Hierarchy Checker

1. Select layer pairs from your derivation sequence to check for overlaps across cell boundaries (hierarchy violations) and run the checking.

2. Explore improper overlaps found for specified layer pairs.

3. Select cells to explode from the list of cells that imply hierarchy violations.
SPICE Output

- Select device parameters for SPICE output
  - MOSFET source/drain attributes
  - Capacitor geometric attributes
  - MOSFET stress effect parameters
  - Resistor geometric attributes

- Output hierarchical and flat SPICE netlists
  - Also output flat netlist when available

Guardian NET Layout Netlist Extractor
Backannotation

- Input schematic file to run Guardian LVS and save relationships between schematic and layout names after the extraction is done
- Use default or custom settings for Guardian LVS

- Used by HIPEX for further schematic backannotation with parasitic devices
Technology Definition

- Define derived layers interactively or use Guardian DRC script
- Use native technology files or setup layer connectivity and design devices interactively
- Convert foreign technology files into native format
- Supports Dracula, Calibre, and Diva rule files
Connectivity Definition

- Soft layers defined on the ERC Setup page have special icon
- Connection to a soft layer is a soft connection. It is unidirectional passing of nodal information to the soft layer
- Use Attach operation for connecting only text labels from an original layer to a conductor layer
- Select contact layer and specify layers it connects by push button clicks
Device Definition

- Extracts all the standard devices: MOSFET, BJT, JFET, MESFET, resistor, capacitor, diode
- Use black boxes (custom devices and subcircuits) to speed up the extraction
- Set device properties, such as sheet resistance for resistors and area and perimeter factors for capacitors, to extract geometry-dependent device parameters
- Supports the third substrate pin for the passive devices and diodes
- Supports multi-terminal resistors and multi-collector and multi-emitter BJTs
Node Probing

- Click layout object to highlight electrical node that object belongs to
- Select two points on the highlighted node to show the shortest connection path between them (Short Locator)
- Zoom to the node object
- Zoom to the entire node
- Show the node object descriptor
- Select the node object for editing
- Select all the node objects for editing
- Navigate through the node objects
- Edit-in-place the cell containing the node object
- Edit the cell containing the node object in a separate window
- Reextract connectivity. Edit and probe nodes on the fly

- Shows node type: net, device, or instance
- Node name in the top cell of the node
- Node name in the lower cell containing the current object of the node
- Layer of the node object
- Hierarchical path through cell instance to the node object
Node Search

- Input net, device, or instance name from the extracted SPICE netlist to highlight
- Specify full hierarchical path to search local nodes below the current cell. Use the colon to separate names of nested instances
Short Locator

The shortest connection path between the selected points shows the short location.

1-left click
2-left click
3-right click

Node 1
Node 2
Short
Conclusion

• Extracts netlists from hierarchical deep submicron IC designs with high level of accuracy and capacity
• The hierarchical engine generates netlists preserving design hierarchy for easy analysis
• Design style and methodology independent. Doesn’t require cell ports for hierarchical extraction
• Provides fast built-in methods for accurate parameter extraction for all the standard devices: MOSFET, BJT, MESFET, JFET, capacitors, resistors, and diodes
• Allows users to make iterative verification runs very quickly through direct invocation from Expert Layout Editor
• Allows interactive definition of extraction settings and rules through user-friendly graphical interface
• Allows node highlighting and inspection in the Expert window
• Performs short isolation
• The integration to Guardian DRC/LVS and HIPEX parasitic extractors within Expert IC design environment provides single-platform verification flow