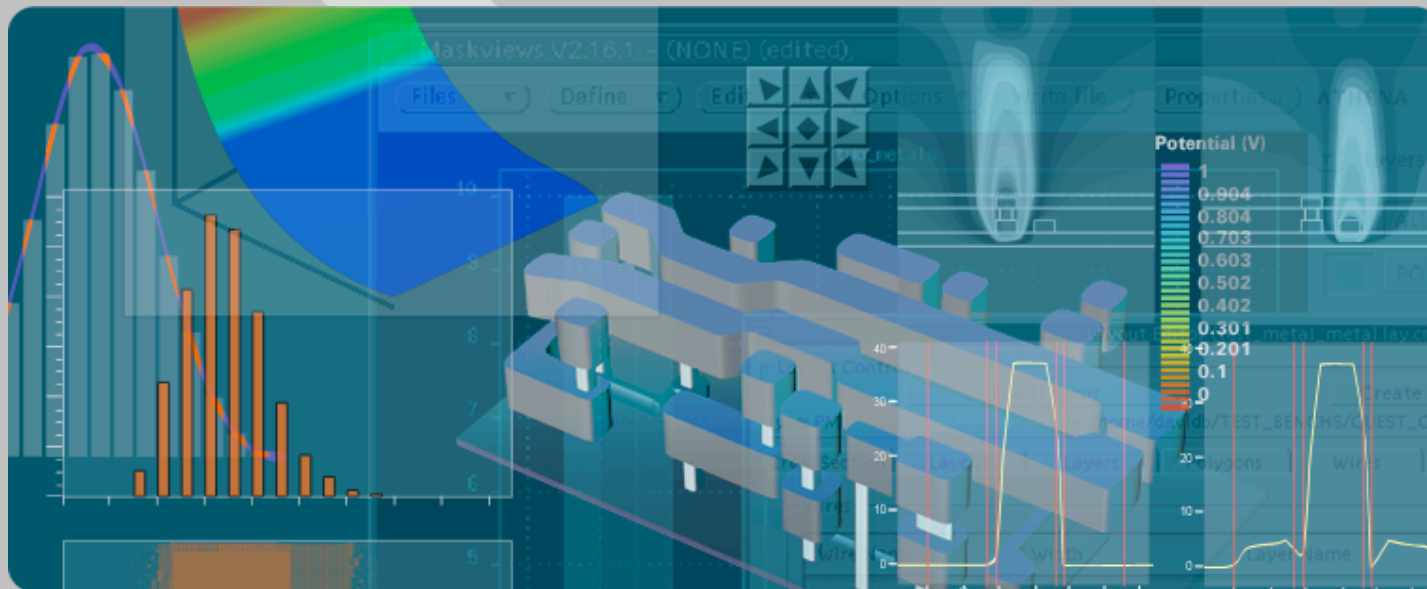# CLEVER Typical Applications

Process Technology Based Extraction and
Optimization of Custom Cell Parasitics

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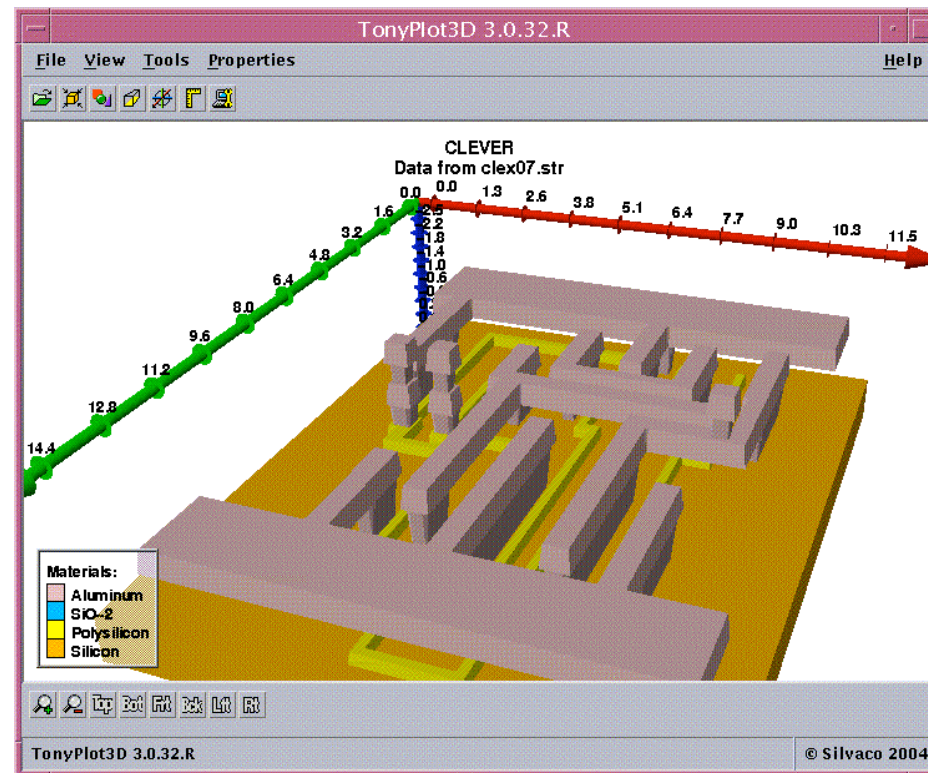
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Exclusive NOR Cell Application

Figure 1. Accurate parasitic extraction for an exclusive NOR cell requires realistic interconnect geometries.

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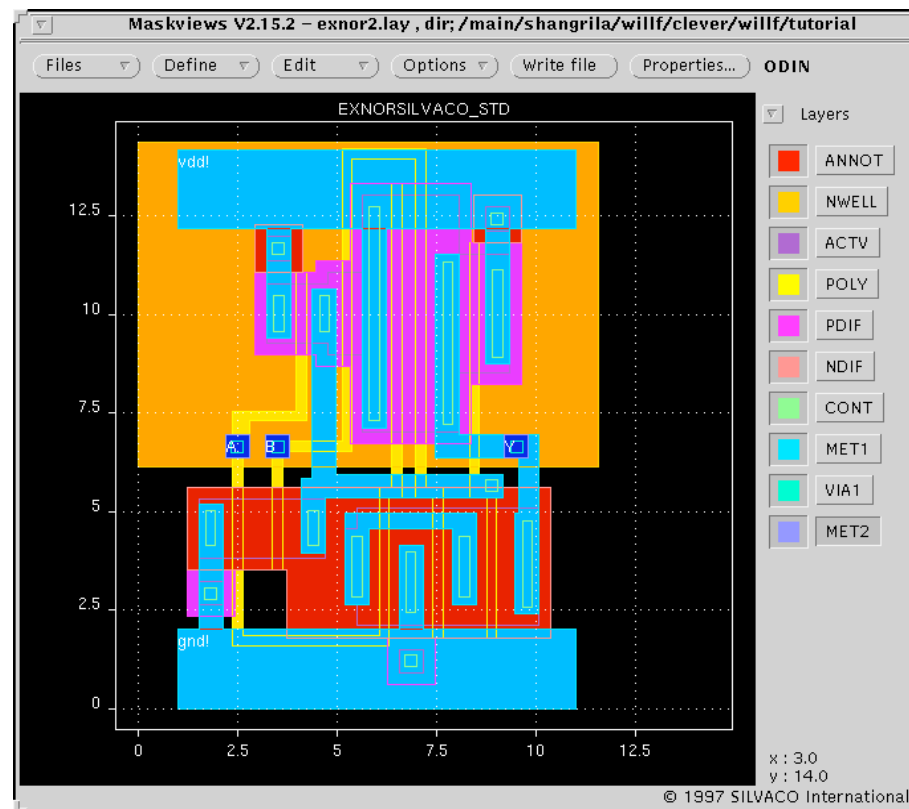# Exclusive NOR Cell Application (con't)

Figure 2. Original GDS-II layout of exclusive NOR cell.
Node labels are read from GDS-II file.
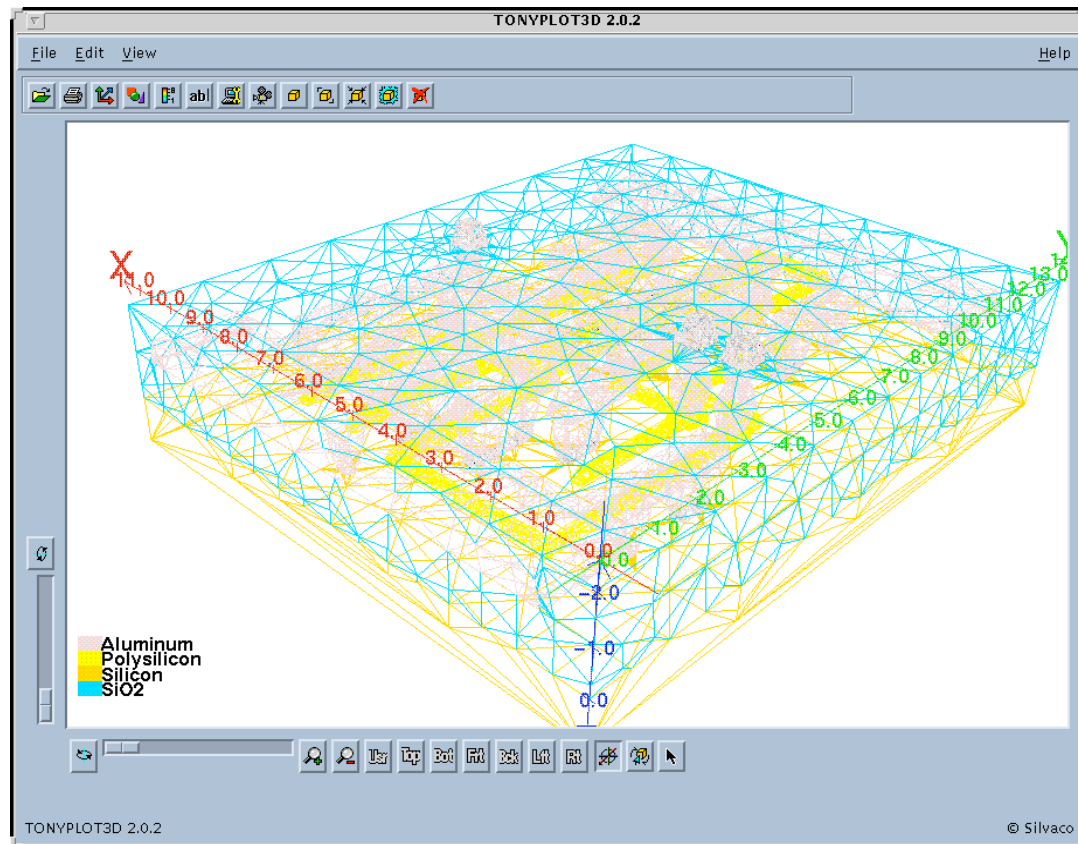
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Exclusive NOR Cell Application (con't)

Figure 3. The 3D adaptive meshing in CLEVER requires no user intervention beyond specifying the desired accuracy of the final parasitics.
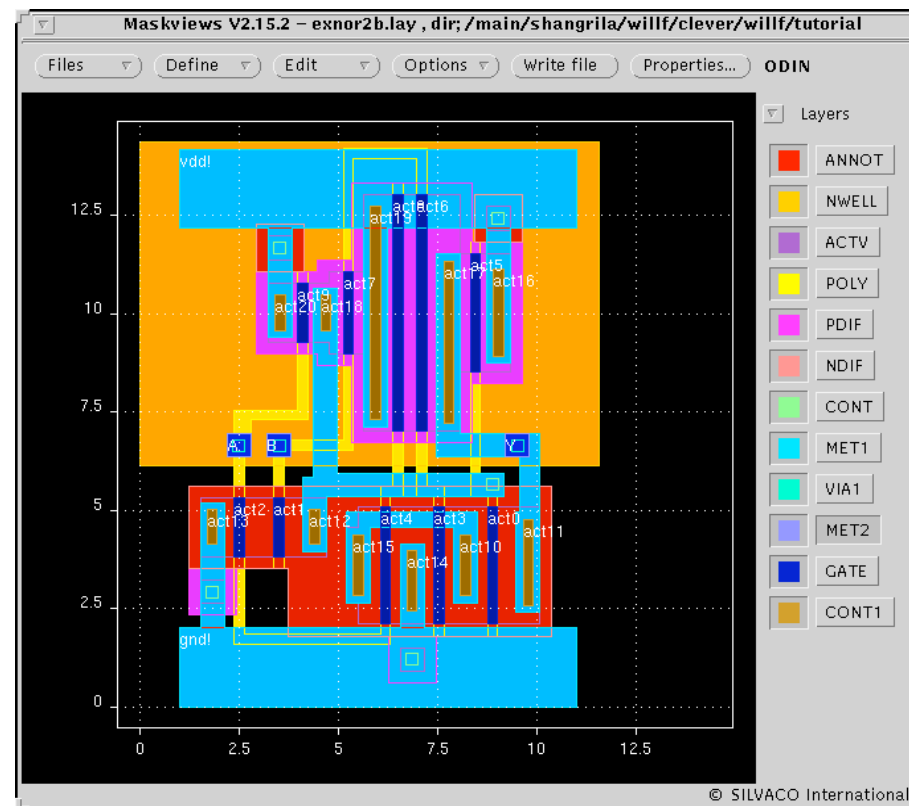
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Exclusive NOR Cell Application (con't)

Figure 4. EXNOR layout annotated with internal node locations.
The internal nodes are used for back-annotation to the netlist.

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Exclusive NOR Cell Application (con't)

Figure 5. Netlist produced by CLEVER includes active devices as well as parasitics. Back-annotation with original node labels is available.

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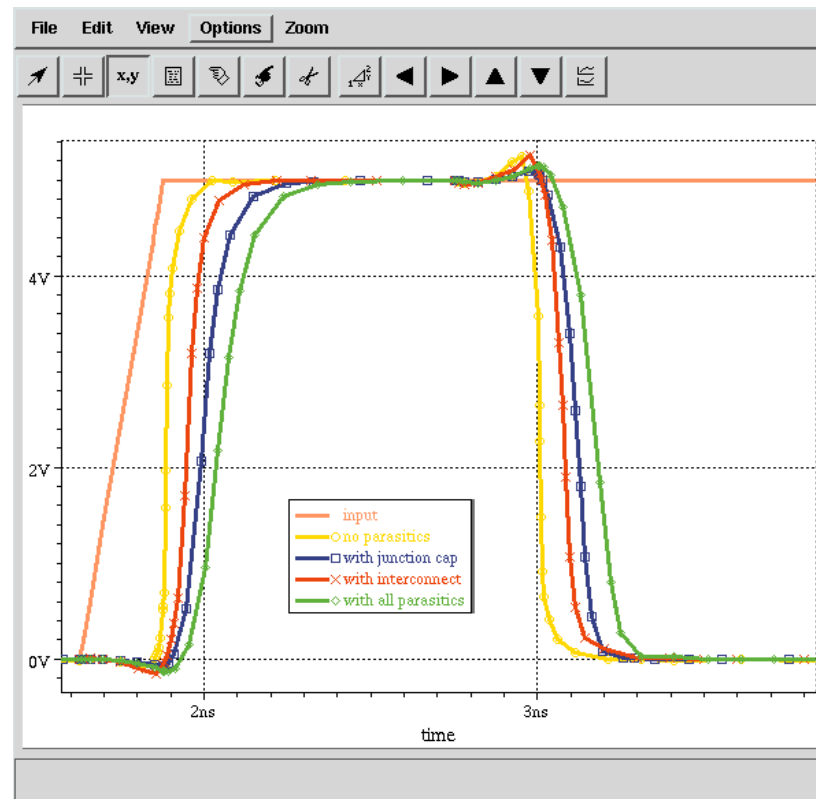# Exclusive NOR Cell Application (con't)

Figure 6. SPICE simulation showing the effect of
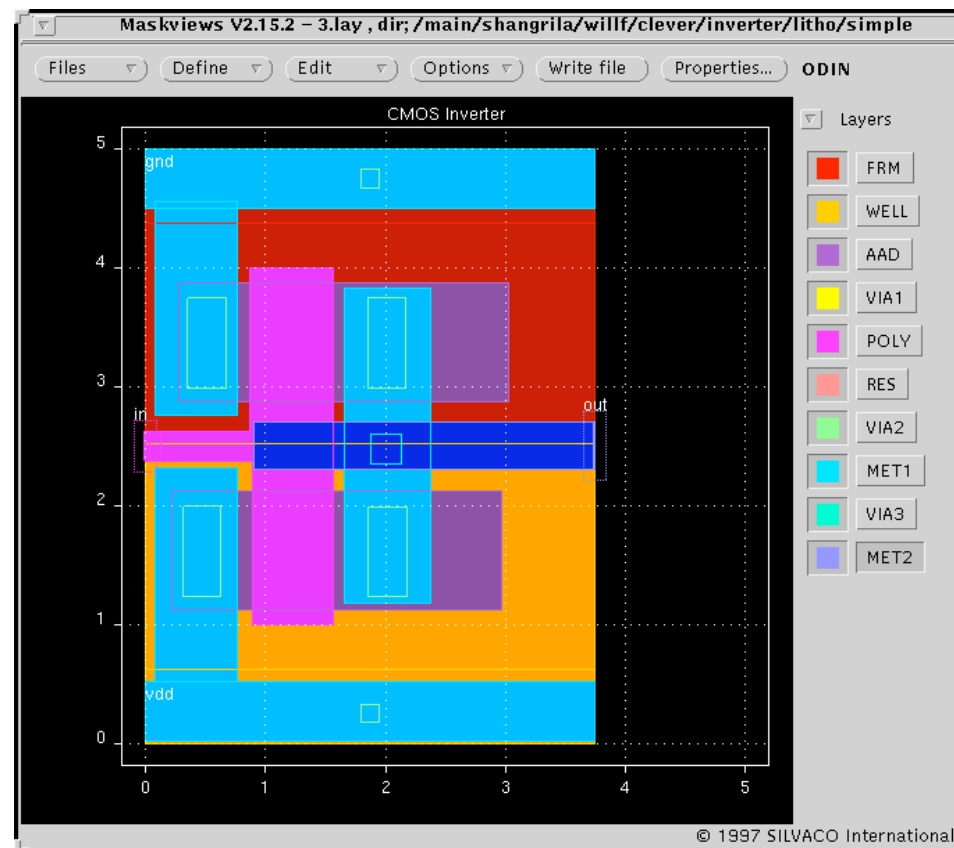interconnect parasitics on timing of the EXNOR cell.

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CMOS Inverter Application

Figure 7. CMOS inverter layout used to compare different interconnect geometry models.
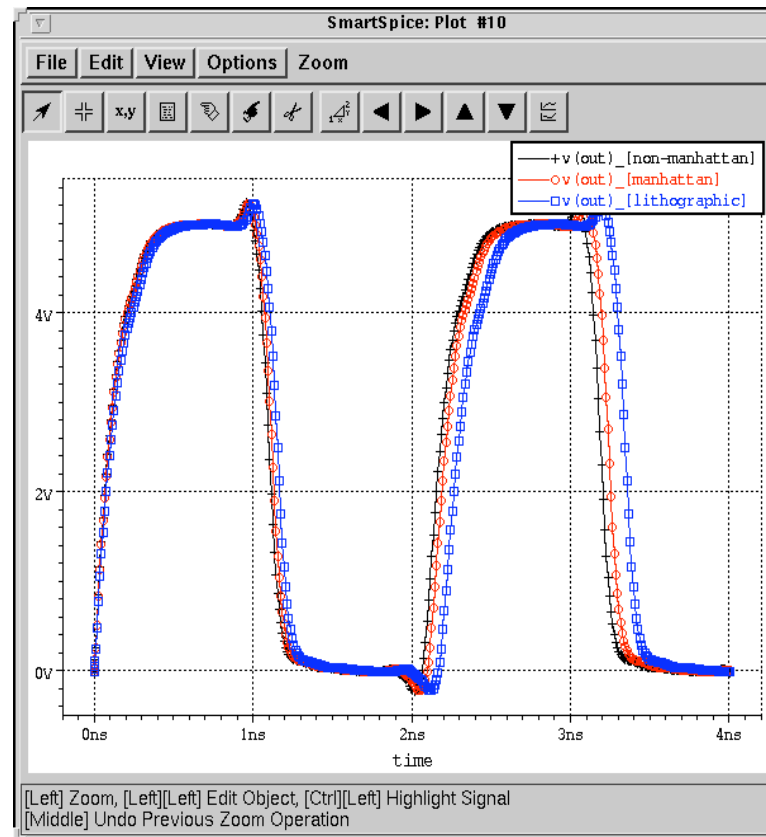
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CMOS Inverter Application (con't)

Figure 8. Effect of using idealized geometries vs. realistic interconnect process simulation on ring oscillator gate delay.

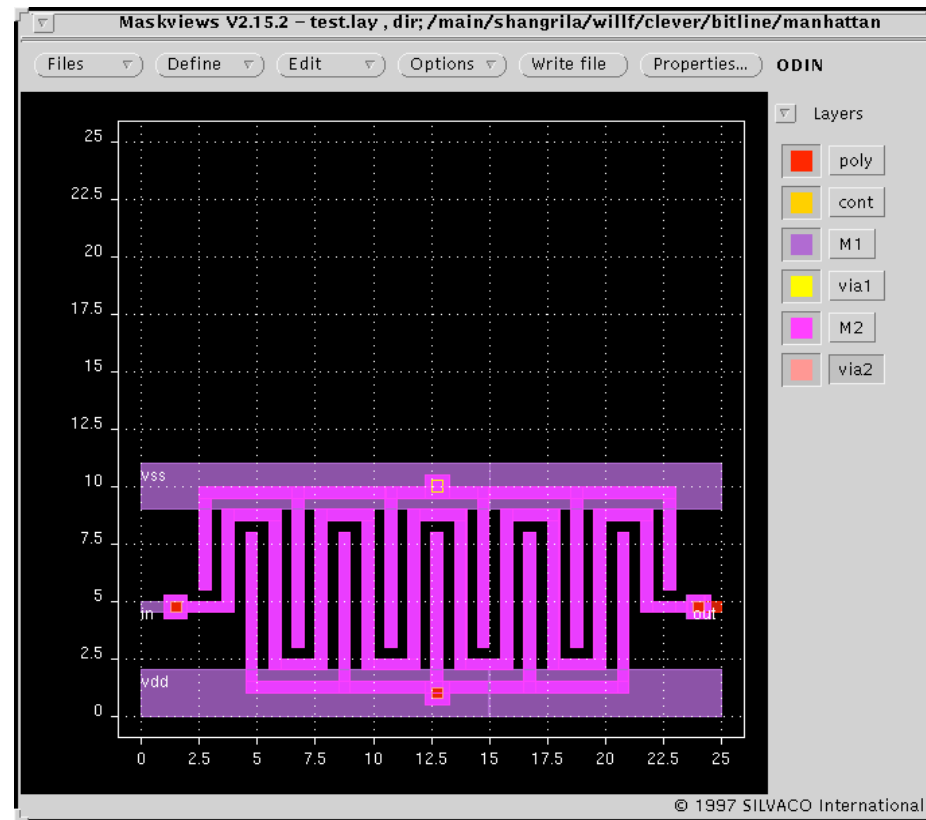**SILVACO**

CMOS Inverter Application (con't)

Figure 9. Metal serpentine used to examine metal width effects.

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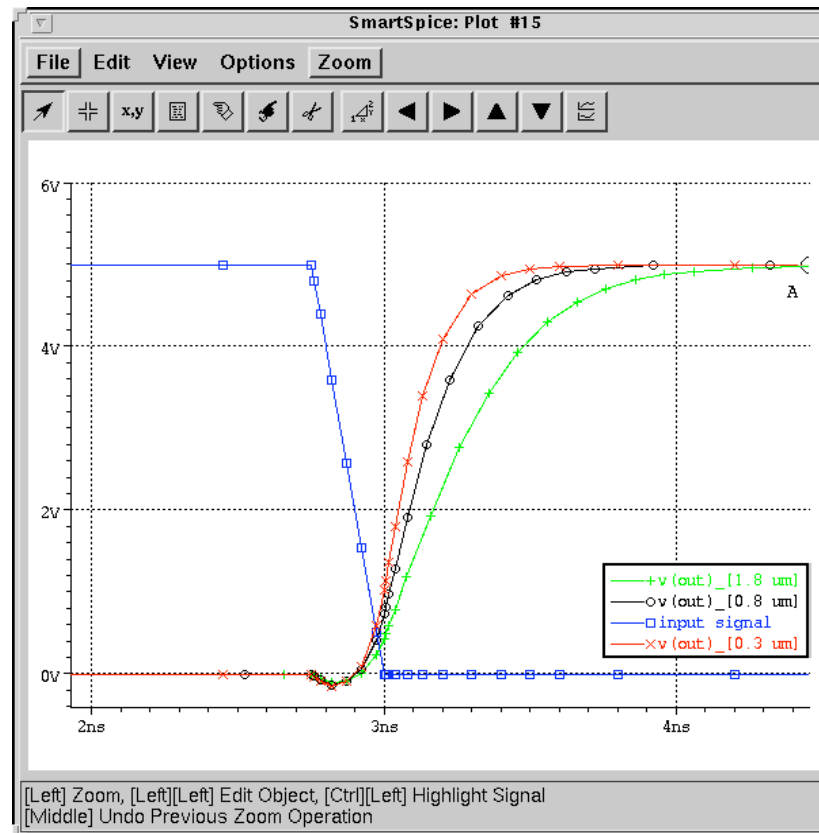# CMOS Inverter Application (con't)

Figure 10. Effects of different metal widths on inverter's gate delay are plotted.
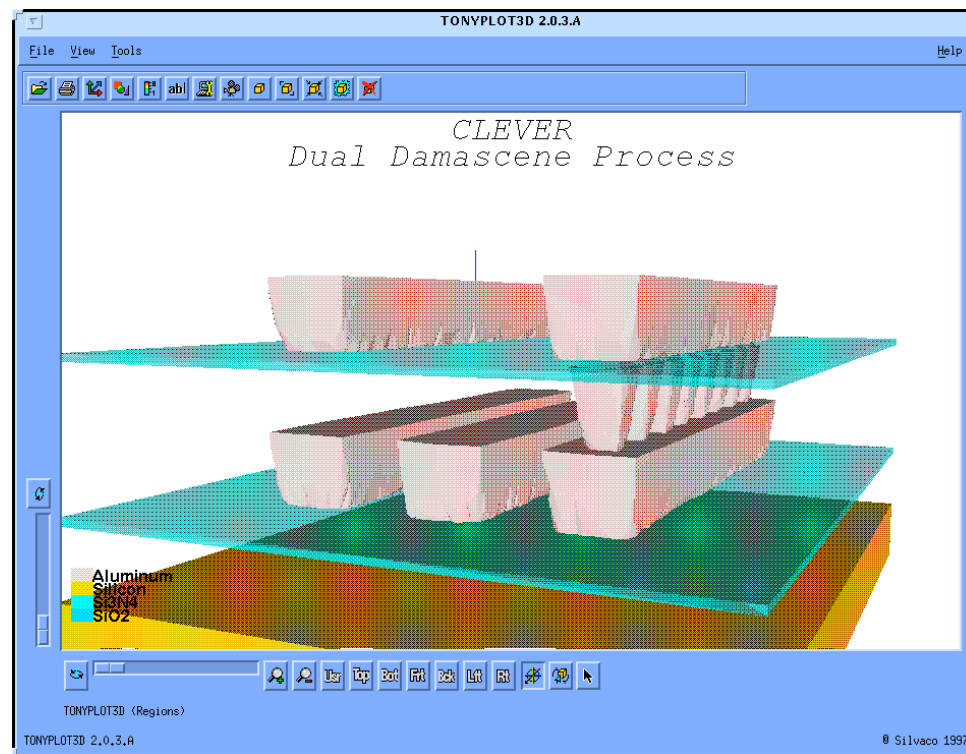
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CMOS Inverter Application (con't)

Figure 11. Simulation of Aluminum Dual Damascene process with nitride etch stops. Clever can handle arbitrary process complexity.
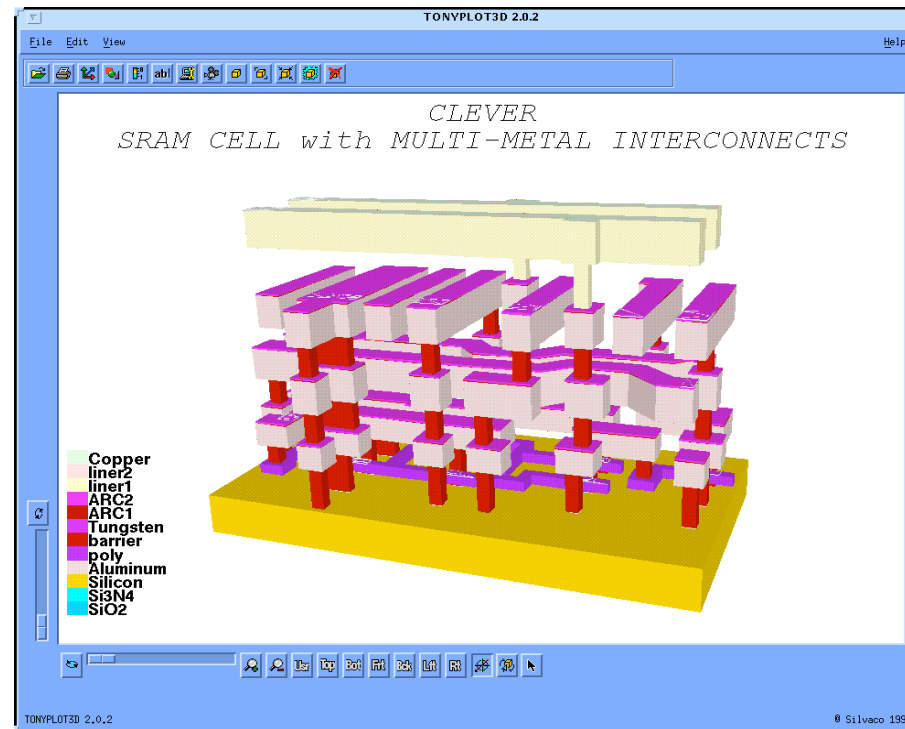
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SRAM Application

Figure 12. SRAM cell with 4 metal layers plus polysilicon. Each metal layer is composed of multiple material layers which are correctly modeled by CLEVER for accurate resistance extraction.

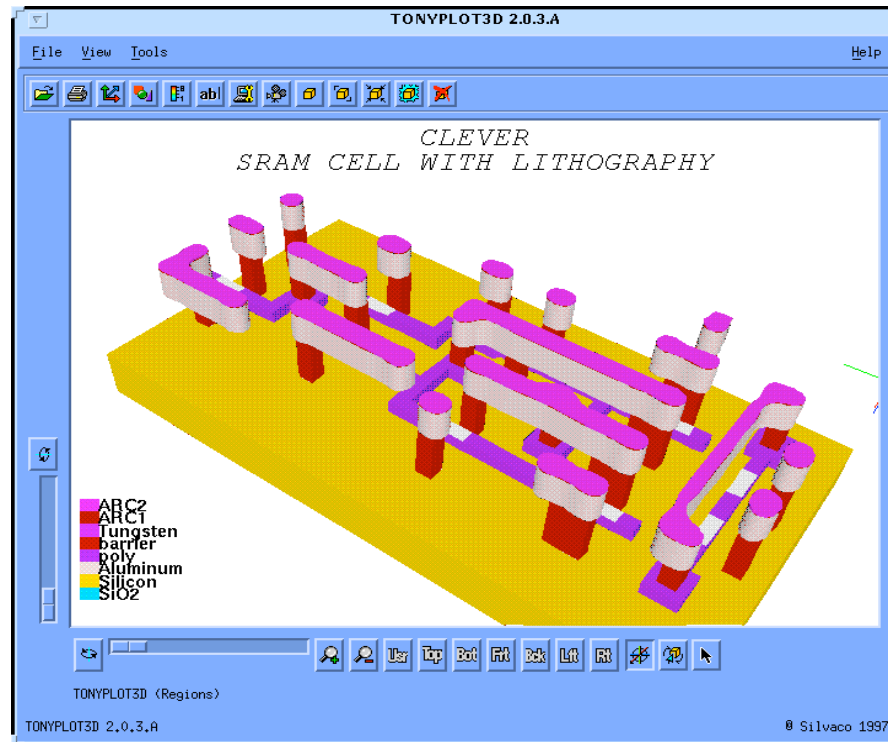**SILVACO**

SRAM Application (con't)

Figure 13. Lithography effect on Metal 1 geometry of an SRAM cell. Significant differences in metal geometry versus an idealized case are seen affecting both capacitance and resistance.

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Conclusion

- CLEVER can be used to examine and optimize interconnect processing and layout effects on circuit timing for any arbitrary small cells

- Full photolithographic and 3D processing capability coupled with the use of field solvers results in the highest possible accuracy for cell level R.C. extraction

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