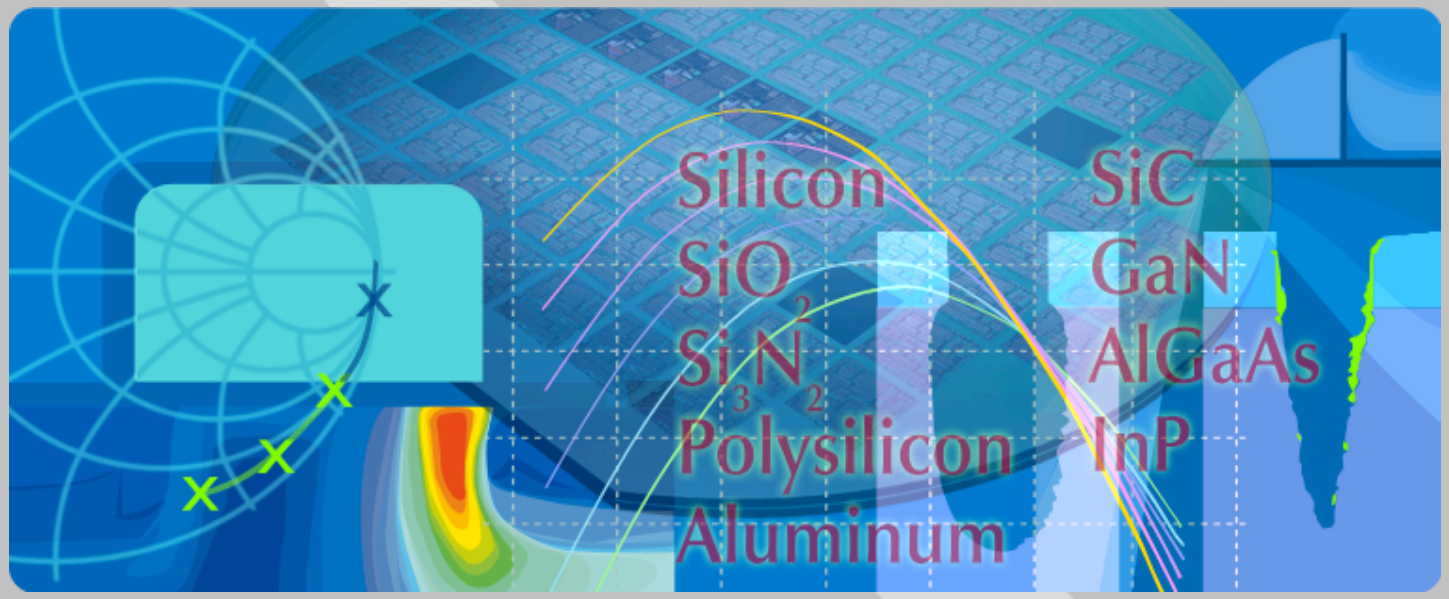
# Workshop on CCD Process and Device Simulation

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# Introduction

- Processing of CCD devices using the ATHENA 2D process simulation framework (SSuprem4)
- Electrical characteristics of CCDs using the ATLAS 2D device simulation framework (S-Pisces)
- Optical characteristics of CCDs using the ATLAS 2D device simulation framework (Luminous)
- Fully integrated simulation environment

# Process Simulation

- ATHENA framework with SSuprem4
- Elite is available for topological deposition and etch models
- Low dose implants
- Local oxidation
- Polysilicon diffusion

# Simulations Applications

- ATLAS framework with S-Pisces and Luminous
- 2D Electrical and Optical Characterization
- DC, Transient and AC solutions
- Dark current and direct Quasi Fermi Level setting modeled
- Terminal currents and “structure” files generated

# Structure Specification

- ATHENA directly transfers:
  - Mesh, Region, Electrode and Doping
- Remeshing with DevEdit is possible if required
- DevEdit and ATLAS internal syntax are alternatives for testing structures

# Material - Models Specification

- Material Parameters
  - Minority carrier lifetimes
- Contact - workfunction of polysilicon
- Interface - fixed charge between oxide and semiconductor
- Models
  - Mobility
    - (recommend CVT field-dependent mobility and concentration-dependent mobility with surface mobility degradation)
  - Recombination
    - Consrh (scales lifetimes to doping)
    - Auger
  - Band gap narrowing (for high concentration areas)

# Light Beam Specification

- “Beam” statement specifies light ray
- Monochromatic or multispectral beams
- Illumination window and beam angle
- Multi beam specification

e.g.

```
beam num=1 wavelength=0.6 x.origin=0 y.origin= -1 \
max.window=2 angle=90
```

# Device Simulation

- Numerical methods - Newton usually OK
- DC optical and electrical calculations
  - e.g. solve b1=1 vdrain=2
- Transient illumination and transient electrical calculations
  - e.g. solve b1=1 ramp.lit ramptime=5e-9 dt=1e-11 tstop=20e-9
- Direct setting of Quasi Fermi Levels (zero carrier mode) with n.bias

# Post-Processing

- Extraction of key parameters
  - Integrated Electron Concentration
  - e.g. extract name="n_conc" 1.0e4*area from curve
    (depth, n.conc material="silicon" mat.occur=1 x.val=1)
  - Line of maximum potential in a structure
  - e.g. extract name="max_p" max.conc.file impurity="potential" \
    x.step=0.01 outfile="max_p.dat"

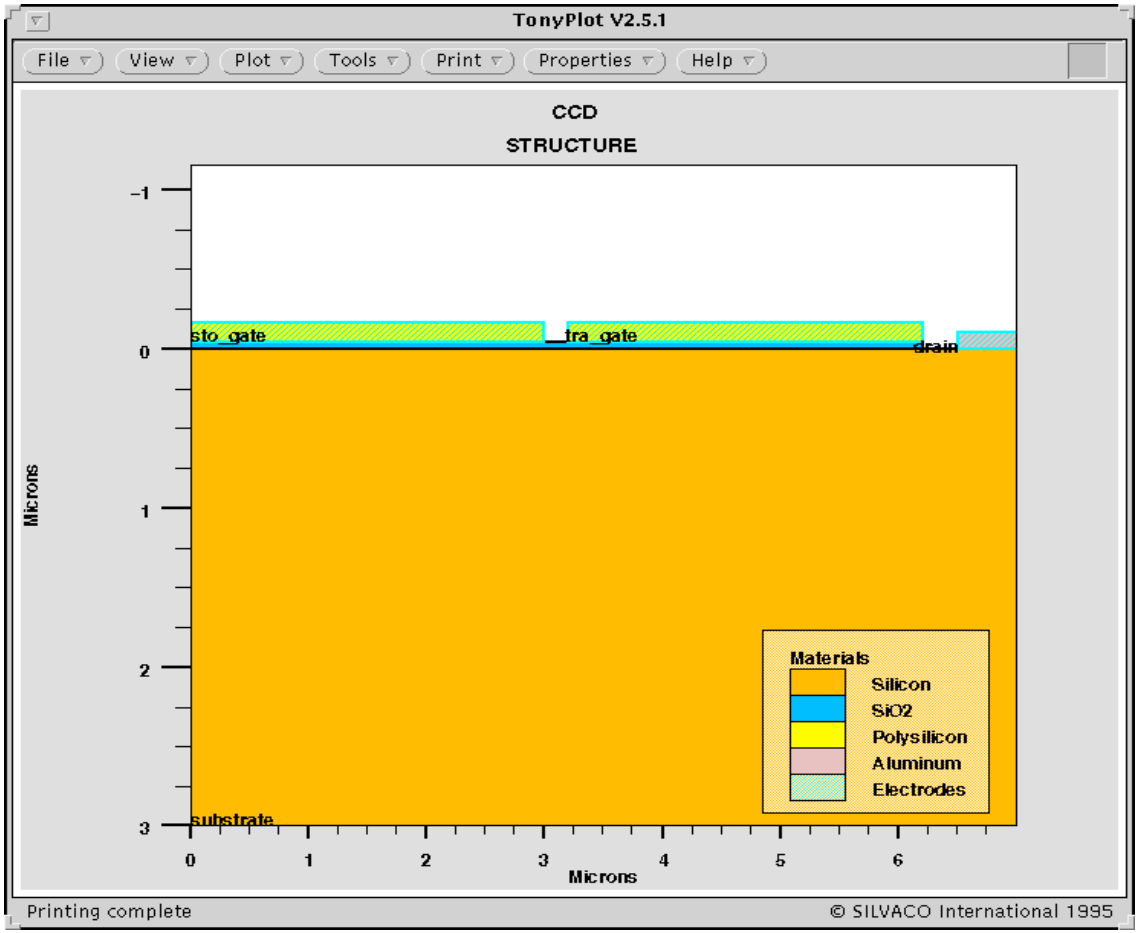
# Example

- Structure generated in ATHENA
  - 3 electrodes (storage, transfer gate and drain)
  - Active n- region implanted at surface
  - p-type substrate
  - Extra p-implant to create potential barrier between storage and transfer gates

# Example

- Empty storage well of carriers
  - Drain at +20V, storage and transfer at -6V
- Illumination with monochromatic beam
  - Transient, 0 - 1 Wcm-2 in 5ns, constant for 15ns, fall
- Charge Transfer from storage to drain
  - Transient, transfer gate ramped from -6V to +2V

# CCD Structure



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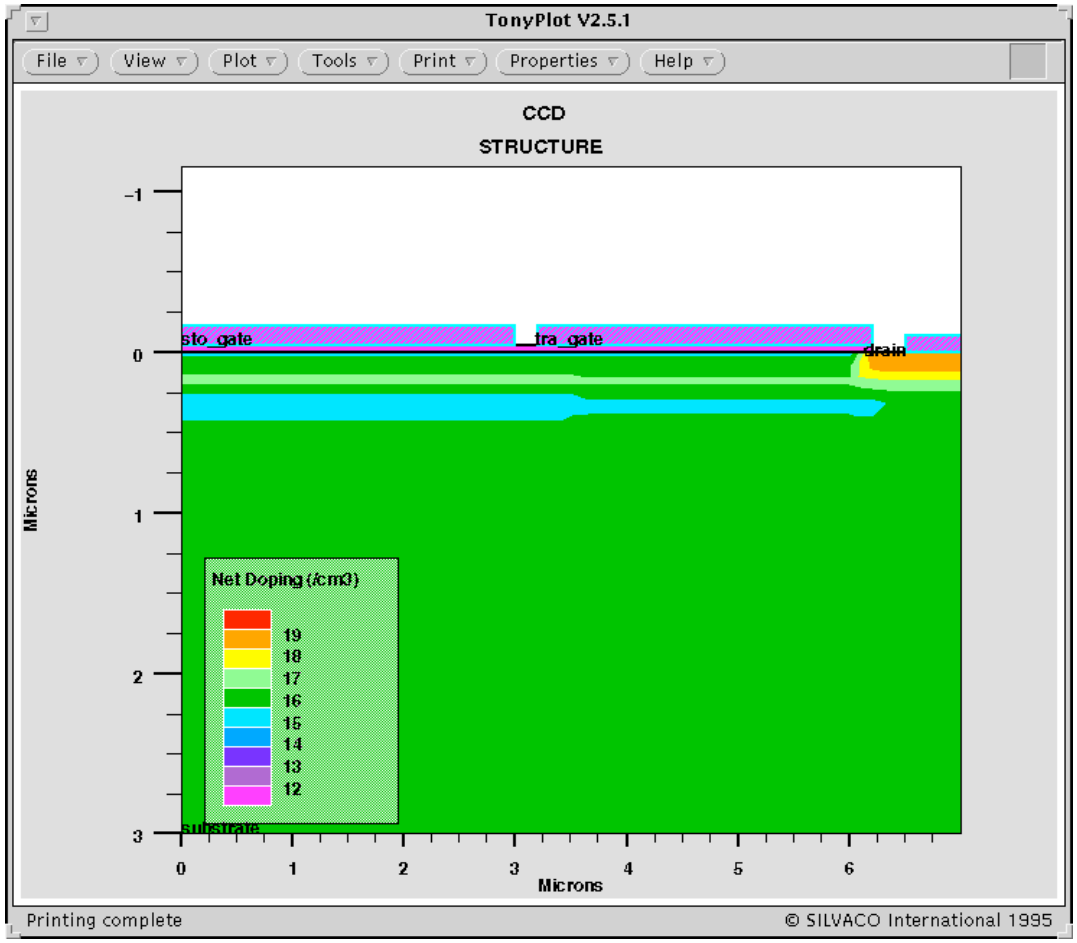
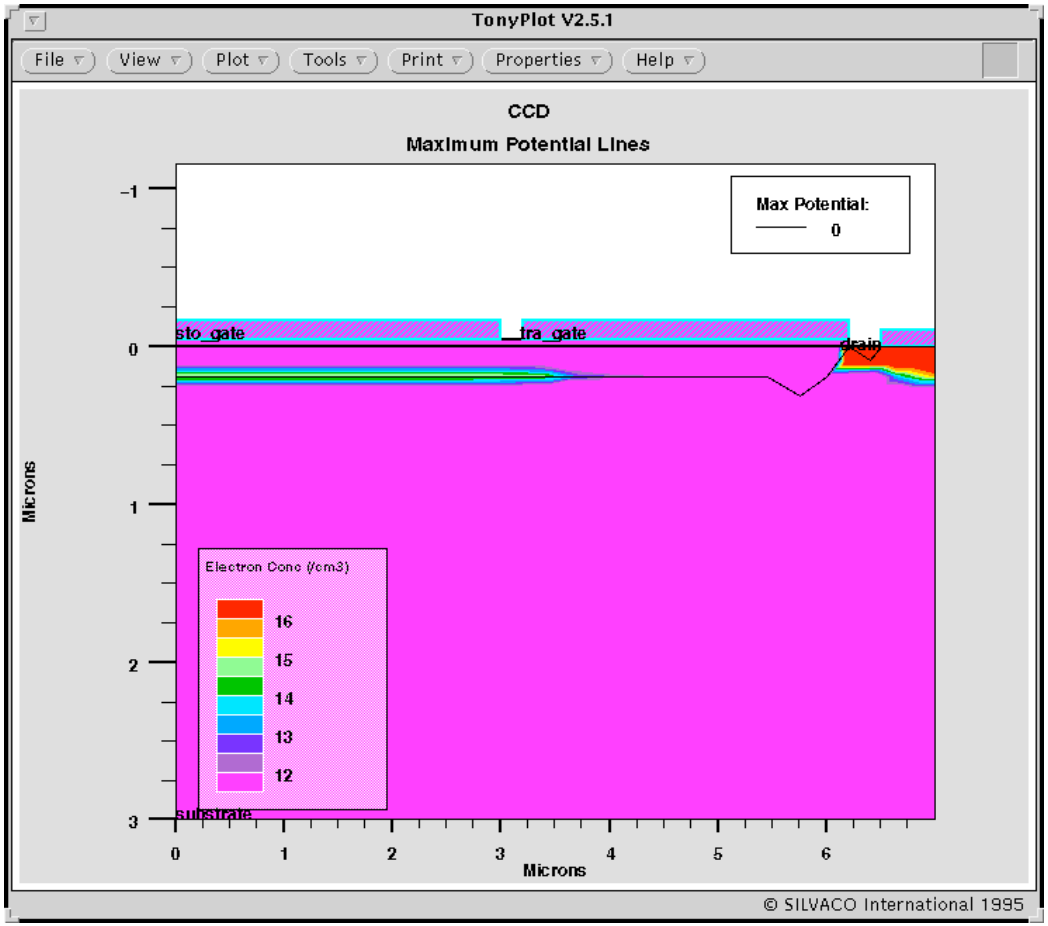
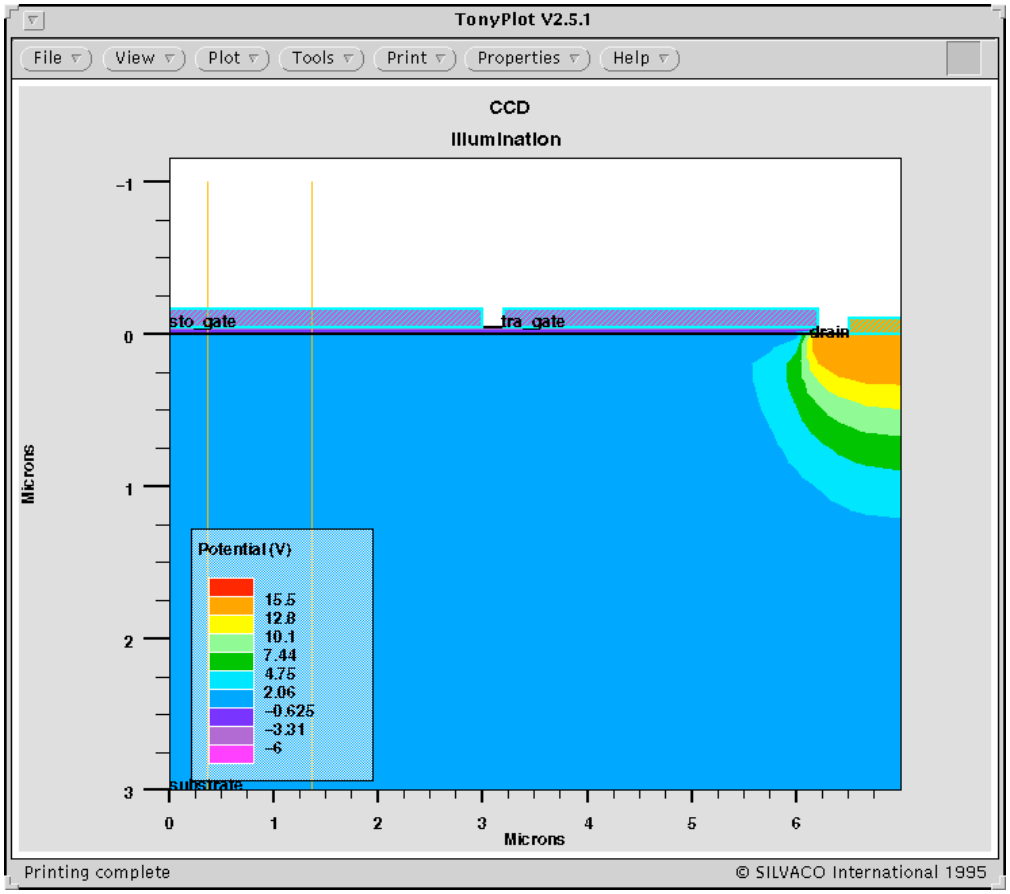


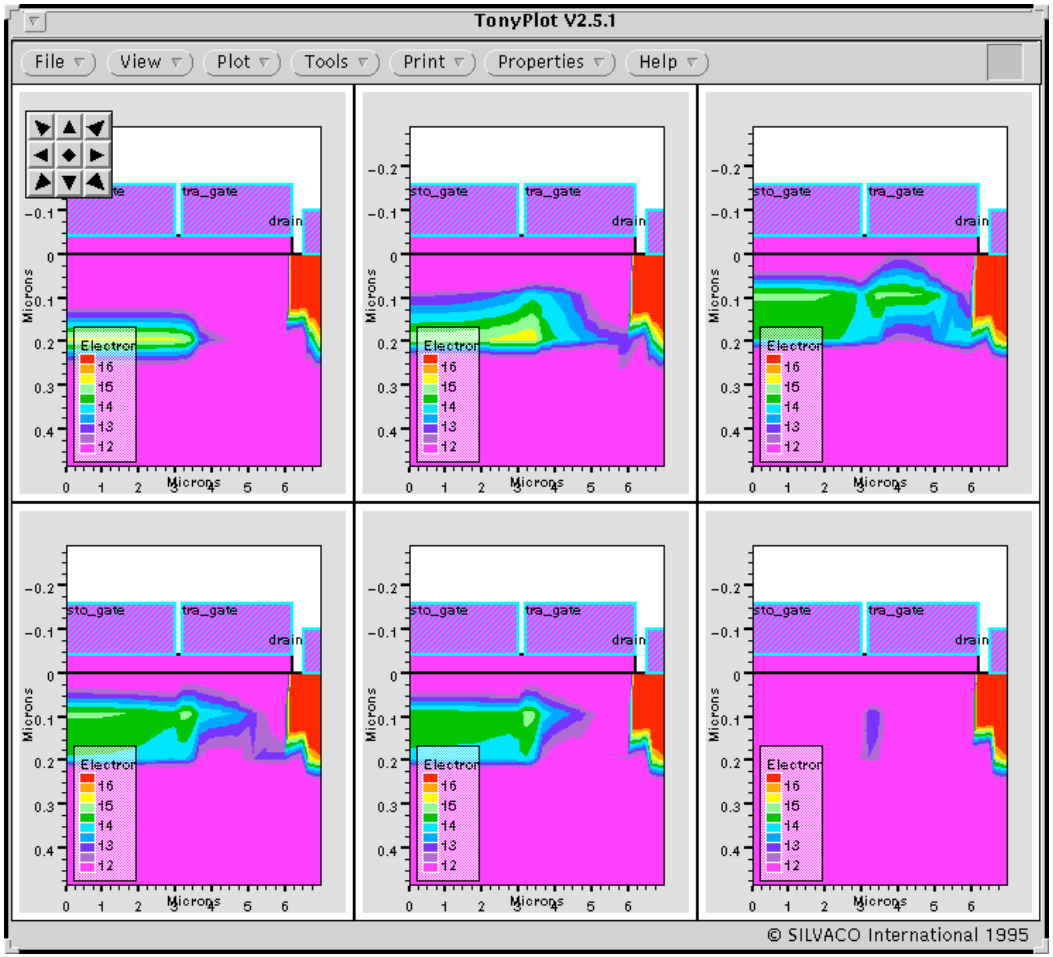
# CCD Maximum Potential Lines



# CCD Illumination



# CCD Device Simulation Movie



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